CM-FX6 CoM

Reference Guide

CompuLab

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CompuLab Ltd.
P.O. Box 687 Yokneam Elite
20692 ISRAEL
Tel: +972 (4) 8290100
http://www.compulab.co.il
Fax: +972 (4) 8325251

Table of Contents

Table 1 Revision Notes

Date	Description
Feb 2013	First release
Jul 2014	1. Update company address. 2. Table 5: changed Active power consumption to "Typ. 2.0 – 6.0 Watt, depending of board configuration, CPU frequency and system load" 3. Table 25: Description of P1-140 (USB1_VBUS) was revised, the phrase "this pin should be left floating" was replaced with "this pin can be left floating" 4. Table 3: Replaced "Boot flash, 1MB" to "Boot flash, 2MB" 5. Table 26: Direction of UART signals revised 6. Chapter 4.10: Added note on UART signal direction control. 7. Table 33: Replaced 'W' option with 'WB' option in availability column. 8. CM-FX6 block diagram fixed: replaced "88MW8787" with "88W8787" 9. Table 40: Removed phrase "Leave unconnected if RTC back-up is not required" 10. Chapter 5.1.1: Added a note on VCC_RTC rail requirements during system start-up. 11. Table 55: minimum main supply voltage changed from 3.6V to 3.3V.

Please check for a newer revision of this manual at the CompuLab web site http://www.compulab.co.il/. Compare the revision notes of the updated manual from the web site with those of the printed or electronic version you have.

1 INTRODUCTION

1.1 About This Document

This document is part of a set of reference documents providing information necessary to operate and program CompuLab CM-FX6 Computer-on-Module.

1.2 CM-FX6 Part Number Legend

Please refer to the CompuLab website 'Ordering information' section to decode the CM-FX6 part number: http://compulab.co.il/products/computer-on-modules/cm-fx6/#ordering.

1.3 Related Documents

For additional information, refer to the documents listed in Table 2.

Table 2 Related Documents

Document	Location
CM-FX6 Developer Resources	http://www.compulab.com/
i.MX6 Reference Manual	http://www.freescale.com/
i.MX6 Datasheet	http://www.freescale.com/

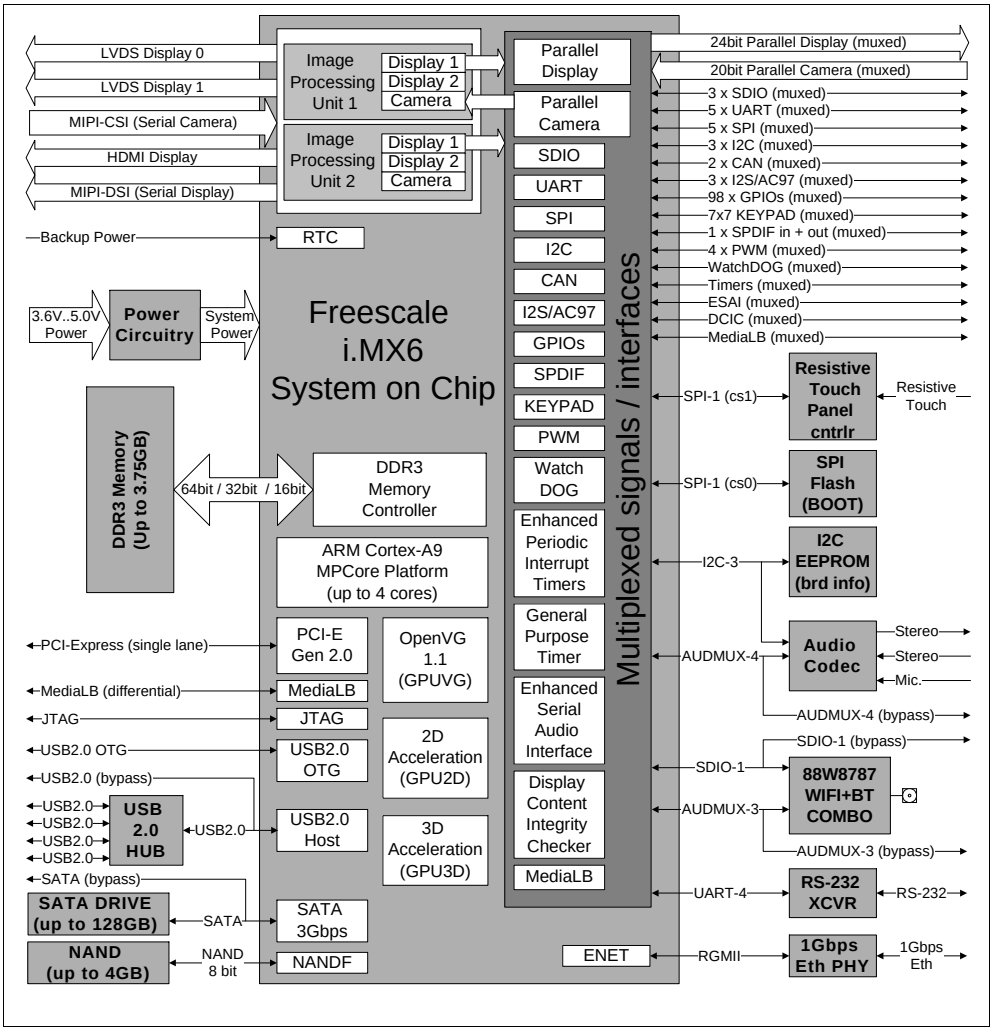
2 OVERVIEW

2.1 Highlights

- Freescale i.MX6 quad-core Cortex-A9 CPU, up to 1.2GHz
- Up to 4GB DDR3
- Up to 32GB on-board SSD storage
- Video Processing Unit, 1080p decoding and encoding
- Integrated GPU with OpenGL-ES and OpenCL EP support
- Graphics controller with up-to 4 display interfaces. Up to 1920 x 1200 resolution
- Gigabit Ethernet, PCI-Express, SATA, USB x5, UART x5, SDIO x3, CAN x2, GPIO x112
- WiFi 802.11b/g/n and Bluetooth 3.0
- Linux, Android ICS and Windows Embedded Compact 7
- Miniature size: 75 x 65 x 8 mm
- SB-FX6 carrier board turns the CM-FX6 module into SBC-FX6 - a single board computer

2.2 Block Diagram

Figure 1 CM-FX6 Block Diagram



2.3 CM-FX6 Features

The "Option" column specifies the configuration code required to have the particular feature. "+" means that the feature is always available.

Table 3 System and Graphics

Feature	Specifications	Option
CPU	Freescale i.MX6 single core Cortex-A9 MPCore™, 1GHz 512KB I/D shared L2 cache; Up to 32-bit DRAM bus width	C1000
	Freescale i.MX6 dual core Cortex-A9 MPCore™, 1GHz 1MB I/D shared L2 cache; Up to 64-bit DRAM bus width	C1000DM
	Freescale i.MX6 quad core Cortex-A9 MPCore™, 1.2GHz 1MB I/D shared L2 cache; Up to 64-bit DRAM bus width	C1200QM
RAM	256MB – 4GB, DDR3-1066, 16-64 bit bus width	D
Storage	Boot flash, 2MB, SPI interface, reprogrammable	+
	On-board NAND flash disk, 128MB - 1GB, 8bit, SLC	N
	On-board SSD, 8GB - 32GB, MLC, through SATA interface	ND ~~C1000~~
Video Processing Unit	Video Processing Unit supports HW decoding/encoding Up to 1080p plus SD 30fps decoding (H.264, VC1, RV10, DivX, etc.) Up to 1080p 30fps encoding (H.264, etc.)	+
Graphics Acceleration Unit	Graphics Processing Unit (GPU3Dv4) compliant with the following standards: OpenGL ES 1.1 and 2.0, OpenVG 1.1, Windows Direct3D, OpenCL EP Graphics Processing Unit (GPU2Dv2) with BitBLT support Vector graphics processing unit (GPUVGv2)	CxxxM

Table 4 I/O

Feature	Specifications	Option
Display	• Parallel 24-bit display interface - up to 225 Mpixels/sec • Two LVDS interfaces. Single port operation support up to 165 Mpixels/sec. Dual port operation supports up to 85 MP/sec for each port • HDMI 1.4 interface • MIPI/DSI, 2 lanes @ 1 Gbps	+
	Simultaneous operation of up to 2 interfaces (total raw pixel rate of up to 225 MPixels/sec at 24 bpp)	C1000
	Simultaneous operation of up to 4 interfaces (total raw pixel rate of up to 450 MPixels/sec at 24 bpp)	CxxxM
USB	1 OTG + 1 host USB2.0 high-speed ports, 480 Mbps	U2
	1 OTG + 4 host USB2.0 high-speed ports, 480 Mbps	U5
SATA	SATA II interface, 3.0 Gbps, integrated controller and PHY	CxxxM ~~ND~~
PCI-Express	PCI Express Gen 2.0 interface	+
Serial Ports (UARTs)	1 RS-232 port, rx/tx only, RS-232 levels (precludes 1 UART port)	+
	Up to 5 UART ports, TIA/EIA-232-F compatible, 3.3V interface, up to 5.0 Mbps	+
CAN bus	Up to 2 CAN bus interfaces (FlexCAN), 3.3V levels	+
Audio	On-board audio codec with analog stereo output, stereo input and electret microphone support	A
	Up to 3 I2S compliant interfaces and enhanced serial audio interface (ESAI)	+
	HDMI audio output and S/PDIF input/output	+
Gigabit Ethernet	1000Base-T Ethernet interface implemented with i.MX6 integrated ENET MAC and the Atheros AR8033 RGMII PHY	E
Camera	1 parallel camera port (up to 20 bit and up to 240 MHz peak) MIPI CSI-2 serial port, supporting from 80 Mbps up to 1 Gbps speed per data lane	+
RTC	Real time clock, powered by external lithium battery	+
Touchscreen Controller	TSC2046 touchscreen controller. Supports 4-wire resistive panels	I
MMC/SD/SDIO	Up to 3 MMC/SD/SDIO interfaces (3V levels), support HC MMC and SDHC up to 32GB:	
	SDIO1 – 1/4 bit transfer modes	~~WB~~
	SDIO2 – 1/4 bit transfer modes	~~A~~
	SDIO3 – 1/4/8bit transfer modes (bootable)	+

WiFi and Bluetooth	Implements 802.11b/g/n wireless connectivity standard Based on Marvell 88W8787. On-board connector for external antenna Bluetooth 3.0 + High Speed (HS) (also compliant with Bluetooth 2.1 + EDR)	WB
General Purpose I/O	Up to 112 multifunction signals. Can be used as GPIO (shared with other functions)	+
I2C	Up to 3 I2C interfaces (up to 400Kbps)	+
SPI	Up to 5 enhanced configurable SPI (eCSPI) bus interfaces (Slave/Master modes)	+

Table 5 Electrical, Mechanical and Environmental Specifications

Supply Voltage	3.3V-5.5V DC
Active power consumption	Typ. 2.0 – 6.0 Watt, depending of board configuration, CPU frequency and system load.
Standby/Sleep consumption	TBD
Dimensions	75 x 65 x 8 mm
Weight	33 gram (w/o Heat-plate)
MTBF	> 100,000 hours
Operation temperature (case)	Commercial: 0° to 70° C Extended: -20° to 70° C Industrial: -40° to 85° C
Storage temperature	-40° to 85° C
Relative humidity	10% to 90% (operation) 05% to 95% (storage)
Shock	50G / 20 ms
Vibration	20G / 0 - 600 Hz
Connectors	2 x 140 pin, 0.6 mm
Connector insertion / removal	50 cycles

3 CORE SYSTEM COMPONENTS

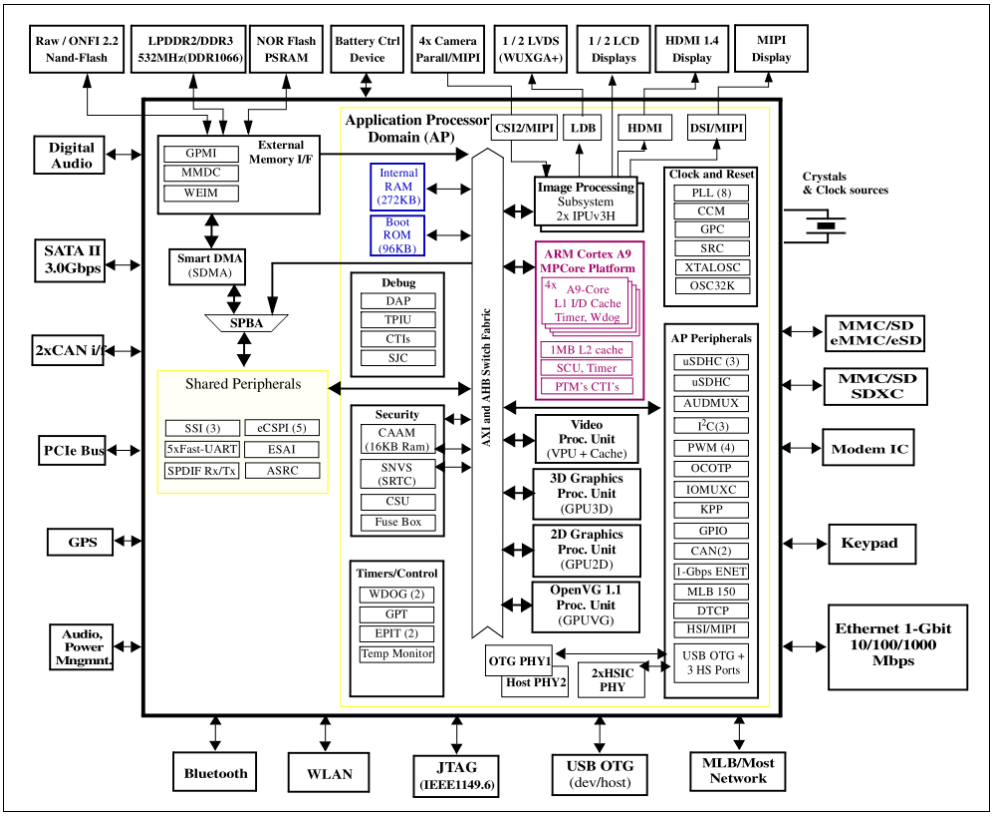
3.1 i.MX6 SoC

The Freescale i.MX6 SoC is an implementation of the quad ARM Cortex™-A9 core, which operates at frequencies up to 1.2 GHz (single and dual core variants are also available). The i.MX6 provides a variety of interfaces and supports the following main features:

- Quad / Dual / Single Core ARM Cortex™-A9. Core configuration is symmetric, where each core includes:
  - 32 KByte L1 Instruction Cache
  - 32 KByte L1 Data Cache
  - Private Timer and Watchdog
  - Cortex-A9 NEON MPE (Media Processing Engine) Co-processor
- Level 2 Cache—Unified instruction and data (up to 1 MByte)
- General Interrupt Controller (GIC) with 128 interrupt support
- Global Timer
- Snoop Control Unit (SCU)
- NEON MPE coprocessor:
  - SIMD Media Processing Architecture
  - NEON register file with 32x64-bit general-purpose registers
  - NEON Integer execute pipeline (ALU, Shift, MAC)
  - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
  - NEON load/store and permute pipeline
- Integrated Power Management unit:
  - Temperature Sensor for monitoring the die temperature
  - DVFS techniques for low power modes
  - Flexible clock gating control scheme
- Multimedia Hardware Accelerators (Optional)

NOTE: Level 2 Cache is limited to 512KByte with the C1000 option of CM-FX6.

Figure 2 i.MX6 (Quad) Block Diagram



3.2 Video and Graphics subsystems

The CM-FX6 video graphics subsystem consists of the following i.MX6 sub-blocks.

- VPU: A multi-standard high performance video codec engine supporting encode/decode operations of the following:
  - Decoding: H.264 BP/CBP/MP/HP, VC-1 SP/MP/AP, MPEG-4 SP/ASP, H.263 P0/P3, MPEG-1/2 MP, Divx (Xvid) HP/PP/HTP/HDP, VP8 (1280x720), AVS, H.264-MVC (1280x720), MJPEG BP (max. 8192x8192) up to full-HD 1920x1088 @30fps plus D1 @30fps.
  - Encoding: H.264 BP/CBP, MPEG-4 SP, H.263 P0/P3, MJPEG BP (max. 192x8192) up to full-HD 1920x1088@30fps.
- GPU3Dv4: A 3D GPU (Vivante GC2000), compliant with OpenGL ES2.0, OpenGL ES1.1 and OpenVG 1.1.
- GPU3Dv5: A 3D GPU (Vivante GC880), compliant with OpenGL ES2.0, OpenGL ES1.1 and OpenVG 1.1.
- GPU2Dv2: Hardware acceleration of 2D graphics (Bit BLT and Stretch BLT). Based on the Vivante GC320 IP core.
- GPUVG: An OpenVG 1.1 Graphics Processing Unit providing hardware acceleration of vector graphics. Based on the Vivante GC355 IP core

NOTE: GPU3Dv5 is not available with the C1000DM and C1200QM options of CM-FX6.

NOTE: GPU3Dv4 and GPUVG are not available with the C1000 option of CM-FX6.

3.3 Memory

3.3.1 DRAM

CM-FX6 is available with up to 4GBytes of DDR3. The DDR3 interface is up to 64-bits wide and operates at up to 533 MHz clock frequencies.

3.3.2 Boot-loader Storage

The CM-FX6 is assembled with 2 MBytes of SPI NOR flash. The SPI NOR flash is the primary non-volatile memory device of CM-FX6, used for the boot-loader and configuration blocks storage.

3.3.3 On-board Storage

CM-FX6 is available with optional secondary on-board storage designed to store the operating system and user data. Any combination of the following on-board non-volatile memory devices can be used as the secondary on-board storage.

- On-board SATA-II SSD (up to 32GBytes).
- On-board raw SLC NAND Flash (up to 1GBytes).

CM-FX6 secondary storage is designed to be used for operating system and general purpose data storage device.

4 PERIPHERAL INTERFACES

CM-FX6 implements a number of peripheral interfaces through the carrier board interface connectors (P1 and P2). The following notes apply to those interfaces:

- Some interfaces/signals are available only with/without certain configuration options of the CM-FX6 CoM. Each signal availability is noted in the "Signals description" table of each interface.
- Many of the CM-FX6 carrier board interface pins are multifunctional. Up-to 8 functions (ALT modes) are accessible through each multifunctional pin. Multifunctional pins are denoted with an asterisk. For additional details, please refer to chapter 5.5.
- Only one multifunctional pin can be used for each function, configuring several multifunctional pins to implement the same function will result in unexpected system behavior.
- All of the CM-FX6 digital interfaces operate at 3.3V voltage levels, unless otherwise noted.

The signals for each interface are described in the "Signal description" tables. The following notes summarize the column headers for these tables:

- **"Signal name"** – The name of each signal with regards to the discussed interface. The signal name corresponds to the relevant function in cases where the carrier board pin in question is multifunctional.
- **"Pin#" –** The carrier board interface pin number where the discussed signal is available, multifunctional pins are denoted with an asterisk.
- **"Type" –** Signal type, see the definition of different signal types below
- **"Description" –** Signal description with regards to the interface in question.
- **"Availability" –** Depending on CM-FX6 Configuration options, certain carrier board interface pins are physically disconnected (floating) on-board CM-FX6. The "Availability" column summarizes configuration requirements for each signal. All the listed requirements must be met (logical AND) for a signal to be "available" unless otherwise noted.

Each described signal can be one of the following types. Signal type is noted in the "Signal description" tables. Multifunctional pin direction, pull resistor and open drain functionality is software controlled. The "Type" column header for multifunctional pins refers to the recommended pin configuration with regards to the discussed signal.

- **"AI"** – Analog Input
- **"AO"** – Analog Output
- **"AIO"** – Analog Input/Output
- **"AP"** – Analog Power Output
- **"I"** – Digital Input
- **"O"** – Digital Output
- **"IO"** – Digital Input/Output
- **"OD"** – Open Drain Signal (not pulled up on-board CM-FX6 unless otherwise noted).
- **"P"** – Power
- "**SPU" –** Software controlled pull up to 3.3V
- "**SPD" –** Software controlled pull down to 3.3V
- **"PU33**" – Always pulled up to 3.3V on-board CM-FX6, (typ. 5KΩ-15KΩ).
- **"PD" -** Always pulled down on-board CM-FX6, (typ. 5KΩ-15KΩ).

4.1 PCI-Express

CM-FX6 is equipped with a single lane PCI Express interface, implemented in the i.MX6 SoC. The PCI Express interface complies with PCIe specification Gen 2.0 and supports the PCI Express 1.1/2.0 standards. The PCI Express module is a dual mode complex, supporting root complex operations and endpoint operations.

The PCI Express module in i.MX6 SoC does not generate the PCI Express ref clock differential signal. The i.MX6 SoC overcomes this limitation by driving a custom generated clock (by means of i.MX6 clock control module) through the i.MX6 LVDS buffered general purpose clock I/O. The LVDS buffered clock can in most cases (where clock jitter requirements are less strict than defined in the PCI-SIG) be used as the PCI Express ref clock. In cases where jitter requirements preclude usage of the LVDS buffered clock, a suitable clock generator must be implemented on the carrier board. Please refer to SB-FX6 for an extensive reference design of PCI-Express ref clock circuitry.

Please refer to chapter 5.4.3 of this document for more details on the i.MX6 general purpose clock IO.

Table 6 PCI-Express signals

Signal Name	Pin #	Type	Description	Availability
PCIE_RXM	P2-106	AI	PCI Express receive data pair	Always available
PCIE_RXP	P2-108	AI		Always available
PCIE_TXM	P2-112	AO	PCI Express transmit data pair	Always available
PCIE_TXP	P2-114	AO		Always available

4.2 Serial ATA Interface

The CM-FX6 incorporates a single SATA-II port implemented with the Freescale i.MX6 integrated SATA controller and PHY. The interface supports the following main features:

- The SATA block fully complies with AHCI specification version 1.10 and partially complies with AHCI specification version 1.3 (FIS-based switching is currently not supported).
- SATA 1.5 Gb/s and SATA 3.0 Gb/s speed.
- Power management features including automatic partial-to-slumber transition.
- eSATA (external analog logic also needs to support eSATA).
- Hardware-assisted Native Command Queuing (NCQ) for up to 32 entries.

Table 7 SATA signals

Signal Name	Pin #	Type	Description	Availability
SATA_RXM	P2-118	AI	SATA receive data pair	Only available **without** 'ND###' options. Only available **without** 'C1000' option.
SATA_RXP	P2-120	AI		Only available **without** 'ND###' options. Only available **without** 'C1000' option.
SATA_TXM	P2-124	AO	SATA transmit data pair	Only available **without** 'ND###' options. Only available **without** 'C1000' option.
SATA_TXP	P2-126	AO		Only available **without** 'ND###' options. Only available **without** 'C1000' option.

4.3 Display and Camera Interfaces

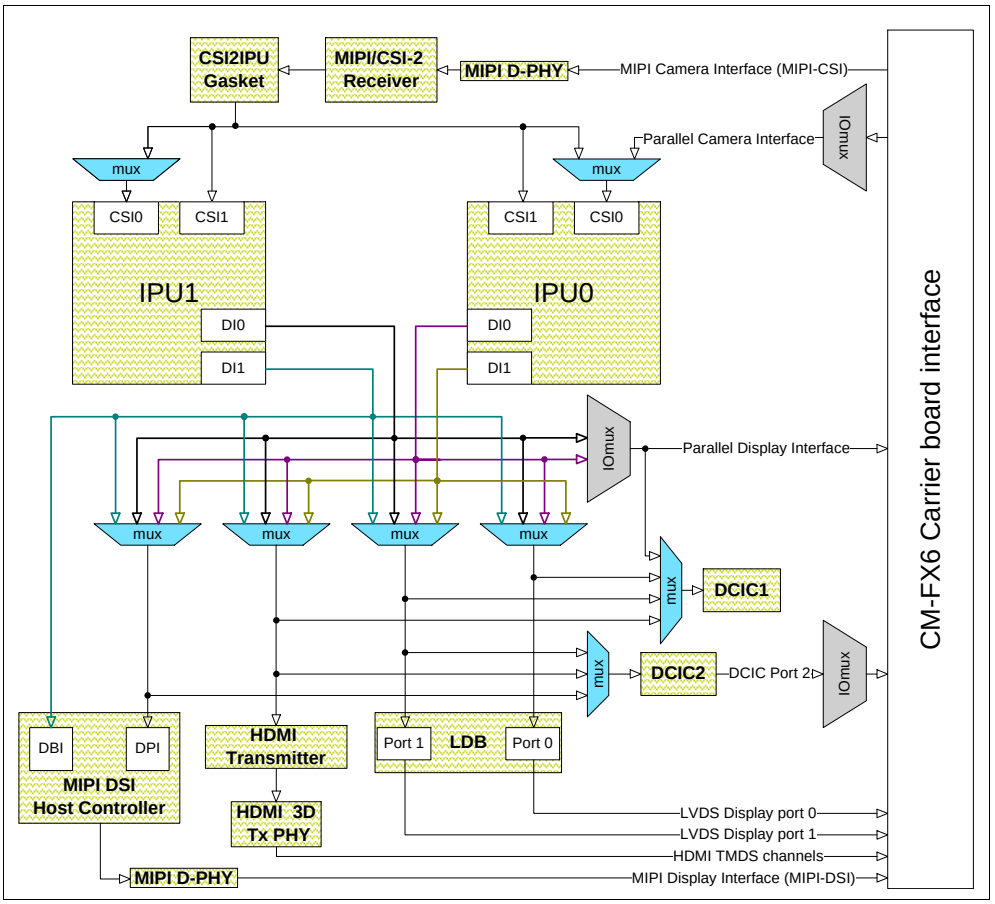
The Display and Camera subsystems of CM-FX6 are derived from the following high level blocks integrated into the i.MX6 SoC:

- Up to 2 Image Processing Units (IPUs) providing connectivity to cameras and displays.
- Display Bridges & Interfaces:
  - MIPI-DSI Host Controller and PHY
  - HDMI Transmitter and PHY.
  - Two port LVDS Display Bridge - LDB
  - Two (identical) Display Content Integrity Checker components (DCIC) designed to authenticate sensitive displayed data.
  - Parallel Display (through IOMUX)
- Camera Bridges & Interfaces:
  - MIPI D-phy, Receiver and CSI2IP Gasket
  - Parallel Camera (through IOMUX)

NOTE: The second IPU is not available with the C1000 option of CM-FX6.

The figure below illustrates the CM-FX6 Display and Camera subsystems high level architecture.

Figure 3 CM-FX6 Display and Camera subsystems architecture



4.3.1 CM-FX6 Display interfaces

The CM-FX6 CoM supports a total of up to 5 display interfaces. The display data flows from system memory into the i.MX6 integrated 'Image Processing Units' (IPUs), where the data is processed and retransmitted into the integrated display bridges (MIPI DSI / HDMI / LDB / Parallel Interface) using the IPU "Display interfaces" (IPU DI1 and DI0).

Figure 3 summarizes the display sources, relevant interfaces and architecture of the CM-FX6 display subsystem.

The i.MX6 SoC can support simultaneous operation of up to 4 displays (up to 2 active IPUs, each driving DI0 and DI1). The following display interfaces are available with CM-FX6:

- A Single Parallel Display interface with up to 200MHz pixel clock frequency
- Two LVDS Display ports with pixel clock rates up to 170MHz
- One HDMI port with pixel clock rates limited by IPU (source of data) to 240MHz max.
- One MIPI/DSI port

The below combinations of displays and max resolution are supported:

- Up to 2 displays: 2 x 4XGA (2048x1536).
- Up to 4 displays: 2 x 1080p (1920x1080) + 2 x WXGA (1280x720).

The following subchapters describe each of the CM-FX6 display interfaces.

NOTE: Only 2 simultaneous displays are supported with the C1000 option of CM-FX6.

4.3.1.1 Parallel Display Interface

The Parallel Display interface of CM-FX6 is derived directly from the DI0 port of the IPU, effectively bypassing all the i.MX6 integrated display bridges (see Figure 3 above).

Each DI port supports the following:

- Compatible with MIPI-DPI standard.
- Supports BT.656 (8-bit) and BT.1120 (16-bit) protocols.
- Supports HDTV standards SMPTE274 (1080i/p) and SMPTE296 (720p)
- Scan Order: progressive or interlaced
- Synchronization:
  - Programmable horizontal and vertical synchronization output signals
  - Data enabling output signal
- The combined data rate for the two DI ports is up to 240 MP/sec
- Supported pixel data formats:
  - RGB - color depth fully configurable; up to 8 bits/value (color component)
  - YUV 4:2:2, 8 bits/value
  - All mandatory formats in MIPI DBI, DPI and DSI

Each of the parallel display interface signals can be sourced either by IPU0 or IPU1 (DI0 port only), the selection between the IPUs is done by means of the IOMUX (please refer to chapter 5.5 of this document for details).

Table 8 Parallel Display Interface signals

Signal Name	Pin #	Type	Description	Availability
LCD interface				
DI0_DISP_CLK	P1-108*	O	Pixel clock	Always available
DI0_PIN2	P1-109*	O	Horizontal synchronization	Always available
DI0_PIN3	P1-107*	O	Vertical synchronization	Always available
DI0_PIN15	P1-105*	O	Data validation/blank, data enable	Always available
DISP0_DAT[0]	P1-75*	O	Pixel data bit 0	Always available
DISP0_DAT[1]	P1-76*	O	Pixel data bit 1	Always available
DISP0_DAT[2]	P1-77*	O	Pixel data bit 2	Always available
DISP0_DAT[3]	P1-78*	O	Pixel data bit 3	Always available
DISP0_DAT[4]	P1-81*	O	Pixel data bit 4	Always available
DISP0_DAT[5]	P1-82*	O	Pixel data bit 5	Always available
DISP0_DAT[6]	P1-83*	O	Pixel data bit 6	Always available
DISP0_DAT[7]	P1-84*	O	Pixel data bit 7	Always available
DISP0_DAT[8]	P1-85*	O	Pixel data bit 8	Always available
DISP0_DAT[9]	P1-87*	O	Pixel data bit 9	Always available
DISP0_DAT[10]	P1-88*	O	Pixel data bit 10	Always available
DISP0_DAT[11]	P1-89*	O	Pixel data bit 11	Always available
DISP0_DAT[12]	P1-90*	O	Pixel data bit 12	Always available
DISP0_DAT[13]	P1-92*	O	Pixel data bit 13	Always available
DISP0_DAT[14]	P1-93*	O	Pixel data bit 14	Always available
DISP0_DAT[15]	P1-94*	O	Pixel data bit 15	Always available
DISP0_DAT[16]	P1-95*	O	Pixel data bit 16	Always available
DISP0_DAT[17]	P1-96*	O	Pixel data bit 17	Always available
DISP0_DAT[18]	P1-97*	O	Pixel data bit 18	Always available
DISP0_DAT[19]	P1-99*	O	Pixel data bit 19	Always available
DISP0_DAT[20]	P1-100*	O	Pixel data bit 20	Always available
DISP0_DAT[21]	P1-101*	O	Pixel data bit 21	Always available
DISP0_DAT[22]	P1-102*	O	Pixel data bit 22	Always available
DISP0_DAT[23]	P1-104*	O	Pixel data bit 23	Always available

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.5 of this document.

NOTE: The "Type" column of Table 8 assumes that this interface is used in "Parallel RGB" mode. Signal type might be different (software controlled) in case a different operation mode is used.

NOTE: The display signal mapping (for example to R[7:0], G[7:0] & B[7:0]) is highly configurable. For examples of valid mappings, please refer to the "IPU Display Interface Signal Mapping" chapter of the i.MX6 datasheet. For detailed information please refer to the "Bus Mapping Unit" chapter of the "i.MX6 Reference Manual".

4.3.1.2 LVDS Display interfaces

The CM-FX6 is equipped with two LVDS Display interfaces. The LVDS Display interfaces are derived from the i.MX6 integrated LVDS Display Bridge (LDB). The main function of the LDB is to transmit display data from the IPU to one or two LVDS interfaced displays (see Figure 3 for LDB integration diagram). The LDB output complies with the EIA-644-A standard and supports the following features:

- Data input interface (inside the i.MX6 SoC)
  - RGB Data of 18 or 24 bits
  - Pixel clock
  - Control signals: HSYNC, VSYNC, DE, and 1 additional optional general purpose control.
- Data output interfaces
  - Single channel output
  - Dual channel output (one input source, two channels outputs for two displays)
  - Split channel output (one input source, 2 channels on output)
  - Separate 2 channel output (2 input sources from IPU).
- Data Rates
  - Overall: LDB supports rates needed by WUXGA 16:10 aspect ratio (1920 x 1200 @ 60 frames per second, data rate supported up to 170 MHz)
  - For single input data interface case: Up to 170 MHz pixel clock (WUXGA 1920x1200)
  - For dual input data interface case: Up to 85 MHz per interface. (WXGA 1366x768 @ 60 frames per second, 35% blanking).

For additional details, please refer to the "LVDS Display Bridge" chapter of the "i.MX 6 Reference Manual".

Table 9 LVDS Display Interfaces signals

Signal Name	Pin #	Type	Description	Availability
LVDS Display port 0				
LVDS0_CLK_N	P1-15	AO	Differential clock pair	Always available
LVDS0_CLK_P	P1-17	AO		
LVDS0_TX0_N	P1-16	AO	Differential data 0 pair	Always available
LVDS0_TX0_P	P1-18	AO		
LVDS0_TX1_N	P1-22	AO	Differential data 1 pair	Always available
LVDS0_TX1_P	P1-24	AO		
LVDS0_TX2_N	P1-28	AO	Differential data 2 pair	Always available
LVDS0_TX2_P	P1-30	AO		
LVDS0_TX3_N	P1-34	AO	Differential data 3 pair	Always available
LVDS0_TX3_P	P1-36	AO		
LVDS Display port 1				
LVDS1_CLK_N	P2-9	AO	Differential clock pair	Always available
LVDS1_CLK_P	P2-11	AO		
LVDS1_TX0_N	P2-28	AO	Differential data 0 pair	Always available
LVDS1_TX0_P	P2-30	AO		
LVDS1_TX1_N	P2-34	AO	Differential data 1 pair	Always available
LVDS1_TX1_P	P2-36	AO		
LVDS1_TX2_N	P2-15	AO	Differential data 2 pair	Always available
LVDS1_TX2_P	P2-17	AO		
LVDS1_TX3_N	P2-21	AO	Differential data 3 pair	Always available
LVDS1_TX3_P	P2-23	AO		

4.3.1.3 MIPI Display Interface

The MIPI Display interface included with CM-FX6 is derived from the i.MX6 integrated MIPI-DSI Host controller. The MIPI-DSI Host controller implements all protocol functions defined in the MIPI-DSI specification, providing an interface between the IPU and the MIPI D-PHY, enabling the communication with a MIPI-DSI compliant display (see Figure 3 for MIPI Display integration diagram). For additional details, please refer to the "MIPI DSI Host Controller" chapter of the "i.MX6 Reference Manual".

The MIPI DSI Host Controller supports the following features:

IPU SIDE (input):

- Compliant with MIPI Alliance Specification for Display Serial Interface (DSI), Version 1.01.00 - 21 February 2008
- Fully Compliant with MIPI Alliance Standard for Display Pixel Interface (DPI-2), Version 2.00 15 September 2005 with Pixel Data bus width up to 24bits
- Compliant with MIPI Alliance Standard for Display Bus Interface (DBI-2) Version 2.00 - 29 November 2005. Supported DBI types are:
  - Type B
  - 16bit, 9bit and 8bit Data bus width
- DBI and DPI interface can coexist (only one is operational at a time)
- Support all commands defined in MIPI Alliance Specification for Display Command Set (DCS), Version 1.02.00 - 23 July 2009

D-PHY side (output):

- Interface with MIPI D-PHY following PHY Protocol Interface (PPI), as defined in MIPI Alliance Specification for D-PHY, Version 1.00.00 - 14 May 2009
- Supports up to 2 D-PHY Data Lanes:
  - Bidirectional Communication and Escape Mode Support through Data Lane 0.
  - Programmable display resolutions, from 160x120(QQVGA) to 1024x768(XVGA).
  - Multiple Peripheral Support capability, configurable Virtual Channels.
  - Video Mode Pixel Formats, 16bpp(RGB565), 18bpp(RGB666) packed, 18bpp(RGB666) loosely, 24bpp(RGB888).

Table 10 MIPI Display Interface signals

Signal Name	Pin #	Type	Description	Availability
LVDS Display port 0				
DSI_CLK_N	P2-81	AO	MIPI Display Differential clock pair	Always available
DSI_CLK_P	P2-83	AO		
DSI_D0_N	P2-105	AO	MIPI Display Differential data 0 pair	Always available
DSI_D0_P	P2-107	AO		
DSI_D1_N	P2-111	AO	MIPI Display Differential data 1 pair	Always available
DSI_D1_P	P2-113	AO		

4.3.1.4 HDMI port

The HDMI port available with CM-FX6 is based on the HDMI transmitter & HDMI 3D Tx PHY integrated into the i.MX6 SoC. Figure 3 shows the video data path from the IPU to the CM-FX6 carrier board interface through the HDMI transmitter & PHY.

Discussing HDMI in the "Display and camera" chapter is not appropriate since in addition to the video/display data from IPU, HDMI transmits audio and control/status data over the TMDS channels. Please refer to chapter 4.4 of this document for further description of HDMI.

4.3.2 Display content integrity checker (DCIC)

The goal of the DCIC is to verify that safety-critical information sent to a display is not corrupted. Such verification is mandatory for warning icons in the instrument cluster of a car, to comply with the ASIL B (Automotive Safety Integrity Level B) specification. It is also required in other safety-sensitive systems. DCIC can monitor either one of the IPU display port outputs or feedback signals going from IO pads of Parallel display interface. Figure 3 shows DCIC integration in CM-FX6.

Each DCIC block can interrupt the ARM complex when data signature calculation is completed and/or a signature mismatch is detected. CM-FX6 also allows notifying an external system (through the carrier board interface) when a signature mismatch is detected in the DCIC2 block.

For additional details, please refer to the "Display Content Integrity Checker" chapter of the "i.MX6 Reference Manual".

Table 11 DCIC2 external indicator signal

Signal Name	Pin #	Type	Description	Availability
DCIC2	P2-47*	O	DCIC2 output signal	Without "**A**" option

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.5 of this document.

4.3.3 Camera Interfaces

Pixel data from an externally connected image sensor or similar device can be transferred into the CM-FX6 system memory by means of the IPU CSI ports and the i.MX6 integrated camera bridges. A total of two camera interfaces are accessible through the CM-FX6 carrier board interface:

- Parallel camera interface (towards IPU0 CSI0 only).
- MIPI/CSI-2 receiver differential interface.

Figure 3 illustrates the pixel data path from the CM-FX6 carrier board interface into the IPU CSI ports. Each IPU accommodates two camera sensor interfaces (CSIs). Each CSI supports both parallel and serial MIPI interfaces. CM-FX6 implementation allows data from the parallel camera interface to be sourced only into the IPU0 CSI0 port, while the data from MIPI/CSI-2 interface can be sourced into any IPU CSI port. Each CSI port supports the following data formats:

- Bayer RGB (8, 9-10 or 11-16 bits per value)
- Full RGB, YUV 4:4:4, YUV 4:2:2
- Grayscale (8 or 16 bits per value)
- Generic Data

For the full list of features, limitations and additional details on the IPU CSI ports please refer to chapter 36.3.1.1 of the "i.MX6 Reference Manual".

The following subchapters describe each of the CM-FX6 camera interfaces.

4.3.3.1 Parallel Camera Interface

The parallel camera interface available with CM-FX6 supports the following features (in addition to the CSI features described in chapter 4.3.2):

- Up-to 20bit input data bus.
- Programmable signal polarity
- Interface Clock frequency of up to 180MHz

Please refer to Figure 3 for a visual illustration of the pixel data path from CM-FX6 carrier board interface into CSI0 port of IPU0 through the parallel camera interface

Table 12 Parallel Camera Interface signals

Signal Name	Pin #	Type	Description	Availability
IPU0_CSI0_PIXCLK	P1-57*	I	Parallel interface pixel clock	Always available
IPU0_CSI0_HSYNC	P1-51*	I	Horizontal synchronization	Always available
IPU0_CSI0_VSYNC	P1-53*	I	Vertical synchronization	Always available
IPU0_CSI0_DATA_EN	P1-59*	I	Data validation/blank, data enable	Always available
IPU0_CSI0_D[0]	P1-40*	I	Parallel input data line 0 [LSB]	Always available
IPU0_CSI0_D[1]	P1-42*	I	Parallel input data line 1	Always available
IPU0_CSI0_D[2]	P1-44*	I	Parallel input data line 2	Always available
IPU0_CSI0_D[3]	P1-46*	I	Parallel input data line 3	Always available
IPU0_CSI0_D[4]	P1-48*	I	Parallel input data line 4	Only available **without** 'WB' option
IPU0_CSI0_D[5]	P1-45*	I	Parallel input data line 5	Only available **without** 'WB' option
IPU0_CSI0_D[6]	P1-47*	I	Parallel input data line 6	Only available **without** 'WB' option
IPU0_CSI0_D[7]	P1-49*	I	Parallel input data line 7	Only available **without** 'WB' option
IPU0_CSI0_D[8]	P1-33*	I	Parallel input data line 8	Always available
IPU0_CSI0_D[9]	P1-35*	I	Parallel input data line 9	Always available
IPU0_CSI0_D[10]	P1-39*	I	Parallel input data line 10	Only available **without** 'WB' option
IPU0_CSI0_D[11]	P1-41*	I	Parallel input data line 11	Only available **without** 'WB' option
IPU0_CSI0_D[12]	P2-64*	I	Parallel input data line 12	Always available
IPU0_CSI0_D[13]	P2-66*	I	Parallel input data line 13	Always available
IPU0_CSI0_D[14]	P2-68*	I	Parallel input data line 14	Always available
IPU0_CSI0_D[15]	P2-70*	I	Parallel input data line 15	Always available
IPU0_CSI0_D[16]	P2-72*	I	Parallel input data line 16	Always available
IPU0_CSI0_D[17]	P2-80*	I	Parallel input data line 17	Always available
IPU0_CSI0_D[18]	P2-82*	I	Parallel input data line 18	Always available
IPU0_CSI0_D[19]	P2-84*	I	Parallel input data line 19 [MSB]	Always available

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.5 of this document.

NOTE: The parallel camera interface signal mapping (for example to R[7:0], G[7:0] & B[7:0]) is data format dependent. For the full signal mapping information please refer to chapter 4.11.9.1 of the i.MX6 datasheet.

4.3.3.2 MIPI camera interface MIPI-CSI

The MIPI camera interface accessible through the CM-FX6 carrier board connectors is basically the receiving section of the i.MX6 integrated MIPI D-PHY block. Serial pixel data sourced from a compliant image sensor and sent over this interface, is de-serialized by the MIPI D-PHY receiver block and re-sent into the IPU trough the MIPI/CSI2 receiver and CSI2IPU bridge. The MIPI/CSI-2 receiver is a digital core that implements all protocol functions defined in the MIPI CSI-2 specification.

Please refer to Figure 3 for a visual illustration of the pixel data path from CM-FX6 carrier board interface into the IPUs through the MIPI camera interface.

The MIPI CSI-2 Receiver supports the following features:

- Compliant with MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2), Version 1.00 - 29 November 2005
- Supports up to 4 Data Lanes
- Dynamically configurable multi-lane merging
- Long and Short packet decoding
- Timing accurate signaling of Frame and Line synchronization packets
- Supports all primary and secondary data formats:
  - RGB, YUV and RAW color space definitions
  - From 24-bit down to 6-bit per pixel
  - Generic or user-defined byte-based data types

For additional details on MIPI-CSI and other relevant system blocks, please refer to chapters 18, 39 and 36.4.3.1 of the “i.MX6 Reference Manual”.

Table 13 MIPI Camera Interface signals

Signal Name	Pin #	Type	Description	Availability
CSI_CLK0M	P2-100	I	Differential MIPI clock input	Always available
CSI_CLK0P	P2-102	I		
CSI_D0M	P2-93	I	Differential MIPI data lane 0 input	Always available
CSI_D0P	P2-95	I		
CSI_D1M	P1-118	I	Differential MIPI data lane 1 input	Always available
CSI_D1P	P1-120	I		
CSI_D2M	P1-121	I	Differential MIPI data lane 2 input	Only available **without** 'C1000' option.
CSI_D2P	P1-123	I		
CSI_D3M	P1-111	I	Differential MIPI data lane 3 input	Only available **without** 'C1000' option.
CSI_D3P	P1-113	I		

4.4 Audio Subsystem

The audio subsystem of CM-FX6 consists of the following two groups of modules:

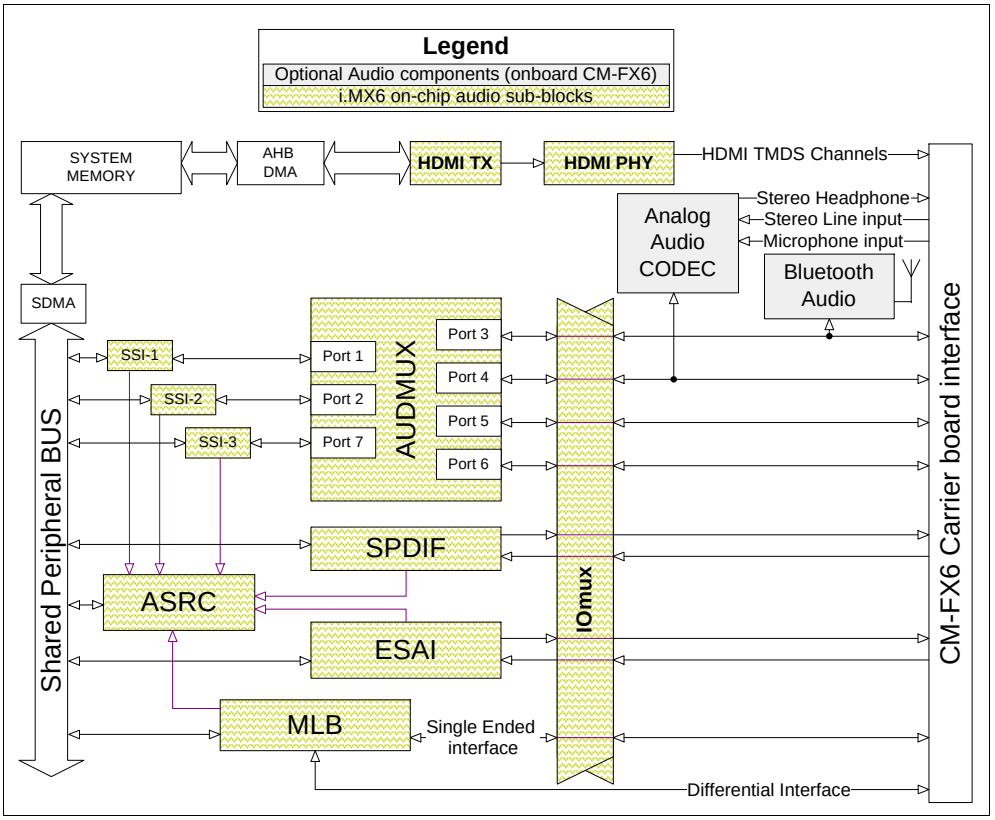
- Internal to the i.MX6 SoC:
  - SSI-1, SSI-2, SSI-3
  - AUDMUX
  - ESAI
  - SPDIF
  - MediaLB
  - HDMI
- External to the I.MX6 SoC (optional, on-board CM-FX6):
  - Analog Audio CODEC
  - Bluetooth Digital Audio (for hands-free applications).

Audio data flows from/to the system memory through an i.MX6 internal bus called the "Shared Peripheral Bus" (see Figure 3). The high level blocks described in the sub-chapters below are designed to transfer audio data between various off-chip devices and the i.MX6 internal "Shared Peripheral BUS".

NOTE: A single special case where audio data path does not involve the "Shared Peripheral Bus" is the when the audio data flows from the system memory into the HDMI TX block, over the i.MX6 AXI bus. Please refer to chapter 4.5 of this document of additional details on HDMI.

A high level overview of the audio subsystem components is shown in Figure 4.

Figure 4 CM-FX6 Audio subsystem architecture



4.4.1 Analog Audio CODEC

The CM-FX6 analog audio functionality is implemented by interfacing the Wolfson WM8731 audio codec with i.MX6 AUDMUX port 4. The Wolfson WM8731 supports the following features:

- Highly Efficient Headphone driver
- Audio performance ('A' weighted): ADC SNR – 90dB, DAC SNR – 100dB.
- Microphone input and electret bias with side tone mixer
- ADC and DAC sampling frequency: 8kHz – 96kHz.
- Selectable ADC high pass filter

The Audio data path from the system memory to the analog audio interface is illustrated in Figure 4.

Table 14 Analog Audio Characteristics

Parameter	Test conditions		Min	Typ	Max	Unit
Stereo Headphone Output						
0-dB full-scale output voltage				1.0		Vrms
Maximum output power, PO	Rload = 32Ω			30		mW
	Rload = 16Ω			50		
Signal-to-noise ratio, A-weighted, (see Notes 1 and 2 below)			90	97		dB
Total harmonic distortion	1kHz output, Rload = 32Ω,	Pout = 10mW rms (-5dB)		0.056 -65	0.1 60	% dB
		Pout = 20mW rms (-2dB)		0.56 -45	1.0 40	% dB
Power supply rejection ratio	1 kHz, 100 mVp-p			50		dB
	20Hz – 20kHz, 100mVpp			45		

Programmable gain	1 kHz output	-73	0	6	dB
Programmable-gain step size	1 kHz		1		dB
Mute attenuation	1 kHz output, 0dB		80		dB
Line Input to ADC					
Input signal level (0 dB)			1.0		Vrms
Signal-to-noise ratio, (see Notes 1 and 2 below)	A-weighted, 0dB gain, Fsample = 48 kHz.	85	90		dB
	A-weighted, 0dB gain, Fsample = 96 kHz.		90		
Dynamic range, (see note 3 below)	A-weighted, −60-dB full-scale input	85	90		dB
Total harmonic distortion	−1-dB input, 0-dB gain		-84 0.006	-74 0.02	dB %
Power supply rejection ratio	1 kHz, 100 mVp-p		50		dB
	20Hz – 20kHz, 100mVpp		45		
ADC Channel Separation	1 kHz input tone		90		dB
Programmable-gain	1 kHz input tone, Rsource<50Ω	-34.5	0	+12	dB
Programmable-gain step size	Guaranteed Monotonic		1.5		dB
Mute attenuation	0dB, 1 kHz input tone		80		dB
Input resistance	12 dB input gain	10	15		kΩ
	0 dB input gain	20	30		
Input capacitance			10		pF
Microphone Input to ADC					
Input signal level (0 dB)			1.0		Vrms
Signal-to-noise ratio, (see Notes 1 and 2)	A-weighted, 0-dB gain		85		dB
Dynamic range, (see Note 3)	A-weighted, −60-dB full-scale input		85		dB
Total harmonic distortion,	0dB input, 0dB gain		-60	-55	dB
Power supply rejection ratio	1 kHz, 100 mVp-p		50		dB
	20Hz – 20kHz, 100mVpp		45		
Programmable-gain Boost	1kHz input, Rsource<50Ω, MICBOOST bit is 1.		34		dB
Mic Path gain (MICBOOST gain is additional to this nominal gain)	MICBOOST bit is 0, Rsource<50Ω,		14		dB
Mute attenuation	0dB, 1 kHz input tone		80		dB
Input resistance			10		kΩ
Input capacitance			10		pF
Microphone Bias					
Bias voltage		2.375	2.475	2.575	V
Bias-current source				3	mA
Output noise voltage	1kHz to 20kHz		25		nV/√Hz

For additional details, please refer to the Wolfson WM8731 datasheet.

Table 15 Analog Audio signals

Signal Name	Pin #	Type	Description	Availability
HP_OUT_R	P2-137	AO	Right channel headphone output	Only available **with** 'A' option.
HP_OUT_L	P2-139	AO	Left channel headphone output	Only available **with** 'A' option.
LINEIN_R	P2-131	AI	Right channel line input	Only available **with** 'A' option.
LINEIN_L	P2-133	AI	Left channel line input	Only available **with** 'A' option.
MIC_IN	P2-129	AI	Microphone input	Only available **with** 'A' option.
MIC_BIAS	P2-125	AP	Electret microphone bias supply	Only available **with** 'A' option.

NOTE: The analog audio codec and interface are only available with the 'A' configuration option.

4.4.2 Digital Audio Interfaces

4.4.2.1 Sony/Philips Digital Interface (S/PDIF)

The CM-FX6 features an S/PDIF interface allowing CM-FX6 to receive and transmit digital audio data. The S/PDIF interface is implemented by means of the i.MX6 integrated S/PDIF transceiver.

The interface is compatible with the Tech 3250-E standard of the European Broadcasting Union, except clause 6.3.3 and the IEC60958-3 Ed2 for relevant topics.

Table 16 summarizes the S/PDIF signals available with CM-FX6.

For additional details, please refer to chapter 57 of the "i.MX6 Reference Manual".

Table 16 S/PDIF signals

Signal Name	Pin #	Type	Description	Availability
SPDIF_OUT	P1-32*	O	S/PDIF transceiver data out	Always available
	P2-104*			Always available
	P2-121*			Always available
SPDIF_IN	P1-116*	I	S/PDIF transceiver data in	Always available
	P1-20*			Always available
	P2-128*			Always available
	P2-27*			Always available

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.5 of this document.

4.4.2.2 Extended Serial Audio Interface (ESAI)

The CM-FX6 features an Enhanced Serial Audio Interface (ESAI), which provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, Sony/Phillips Digital Interface (SPDIF) transceivers and DSPs. The ESAI consists of independent transmitter and receiver sections and supports the following features:

- Independent (asynchronous mode) or shared (synchronous mode) transmit and receive sections with separate or shared internal/external clocks and frame syncs, operating in Master or Slave mode.
- Up to six transmitters and four receivers with TX2/RX3, TX3/RX2, TX4/RX1 and TX5/RX0 pins shared by transmitters 2 to 5 and receivers 0 to 3. TX0 and TX1 pins are used by transmitters 0 and 1 only.
- Programmable data interface modes such as I2S, LSB aligned, MSB aligned
- Programmable word length (8, 12, 16, 20 or 24bits)
- AC97 support
- 128-word Transmit FIFO shared by six transmitters
- 128-word Receive FIFO shared by four receivers

Figure 4 illustrates the ESAI integration with the CM-FX6 audio sub-system. Table 17 summarizes the ESAI signals available with CM-FX6. For additional details, please refer to chapter 24 of the "i.MX6 Reference Manual".

Table 17 ESAI signals

Signal Name	Pin #	Type	Description	Availability
ESAI_FSR	P2-77*	IO	Frame Sync for Receiver	Always available
ESAI_FST	P1-58*	IO	Frame Sync for Transmitter	Always available
	P2-20*			Always available
ESAI_HCKR	P2-128*	IO	High Frequency Clock for Receiver	Always available
ESAI_HCKT	P1-56*	IO	High Frequency Clock for Transmitter	Always available
	P2-121*			Always available
ESAI_SCKR	P2-71*	IO	Receiver Serial Clock	Always available
ESAI_SCKT	P2-89*	IO	Transmitter Serial Clock	Always available
ESAI_TX0	P2-97*	O	Serial transmit 0 data	Always available
ESAI_TX1	P2-119*	O	Serial transmit 1 data	Always available
ESAI_TX2_RX3	P2-39*	IO	Serial transmit 2 / receive 3 data	Always available
	P2-53*			Only available **without** 'A' option.
ESAI_TX3_RX2	P1-20*	IO	Serial transmit 3 / receive 2 data	Always available
ESAI_TX4_RX1	P1-72*	IO	Serial transmit 4 / receive 1 data	Always available
ESAI_TX5_RX0	P1-61*	IO	Serial transmit 5 / receive 0 data	Always available

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.5 of this document.

4.4.2.3 Synchronous Serial Interface (SSI) and Digital Audio Multiplexer (AUDMUX)

CM-FX6 is equipped with three SSI ports. The SSI port is a full-duplex, serial port designed for communication with a variety of devices that implement the inter-IC sound bus standard (I2S) and Intel AC97 standard. The following main features are supported:

- Independent (asynchronous) or shared (synchronous) transmit and receive sections with separate or shared internal/external clocks and frame syncs, operating in master or slave mode
- Normal mode operation using frame sync
- Network mode operation allowing multiple devices to share the port with as many as 32 time slots
- Gated Clock mode operation requiring no frame sync
- 2 sets of Transmit and Receive FIFOs. Each of the four FIFOs is 15x32 bits. The two sets of Tx/Rx FIFOs can be used in Network mode to provide 2 independent channels for transmission and reception
- Programmable data interface modes such as I2S, LSB, MSB aligned
- Programmable word length (8, 10, 12, 16, 18, 20, 22 or 24 bits)
- Program options for frame sync and clock generation
- Programmable I2S modes (Master, Slave or Normal). 8 kHz up to 196 kHz audio sampling rate.
- AC97 support. 8 kHz up to 48 kHz frame rate

The SSI ports are accessible through the "Digital Audio multiplexer" (AUDMUX) block.

AUDMUX enables programmable synchronous data routing between the SSI ports and devices external to the i.MX6 SoC. The CM-FX6 on-board analog audio codec and the bluetooth audio devices communicate with their SSI ports through AUDMUX ports 4 and 3 respectively (see Figure 4). AUDMUX supports the below listed features:

- Three internal ports
- Four external ports

- Full 6-wire SSI interfaces for asynchronous receive and transmit
- Configurable 4-wire (synchronous) or 6-wire (asynchronous) peripheral interfaces
- Independent Tx/Rx Frame sync and clock direction selection for host or peripheral
- Each host interface capability to connect to any other host or peripheral interface in a point-to-point or point-to-multipoint (network mode)

Table 18 summarizes the AUDMUX signals available through the CM-FX6 carrier board interface. For additional details, please refer to chapters 59 and 15 of the "i.MX6 Reference Manual".

Table 18 AUDMUX and SSI signals

Signal Name	Pin #	Type	Description	Availability
AUDMUX port 3				
AUD3_RXC	P1-39*	IO	Clock receive port 3	Only available **without** 'WB' option.
AUD3_RXD	P1-49*	IO	Data receive port 3	Only available **without** 'WB' option.
AUD3_RXFS	P1-41*	IO	Frame sync receive port 3	Only available **without** 'WB' option.
AUD3_TXC	P1-48*	IO	Clock transmit port 3	Only available **without** 'WB' option.
AUD3_TXD	P1-45*	IO	Data transmit port 3	Only available **without** 'WB' option.
AUD3_TXFS	P1-47*	IO	Frame sync transmit port 3	Only available **without** 'WB' option.
AUDMUX port 4				
AUD4_RXC	P1-99*	IO	Clock receive port 4	Only available **without** 'A' option.
	P2-57*			Only available **without** 'A' option.
AUD4_RXD	P1-104*	IO	Data receive port 4	Only available **without** 'A' option.
	P2-47*			Only available **without** 'A' option.
AUD4_RXFS	P1-97*	IO	Frame sync receive port 4	Only available **without** 'A' option.
	P2-59*			Only available **without** 'A' option.
AUD4_TXC	P1-100*	IO	Clock transmit port 4	Only available **without** 'A' option.
	P2-45*			Only available **without** 'A' option.
AUD4_TXD	P1-101*	IO	Data transmit port 4	Only available **without** 'A' option.
	P2-49*			Only available **without** 'A' option.
AUD4_TXFS	P1-102*	IO	Frame sync transmit port 4	Only available **without** 'A' option.
	P2-51*			Only available **without** 'A' option.
AUDMUX port 5				
AUD5_RXC	P1-73*	IO	Clock receive port 5	Always available
	P1-93*			Always available
AUD5_RXD	P1-66*	IO	Data receive port 5	Always available
	P1-99*			Always available
AUD5_RXFS	P1-65*	IO	Frame sync receive port 5	Always available
	P1-92*			Always available
AUD5_TXC	P1-95*	IO	Clock transmit port 5	Always available
AUD5_TXD	P1-96*	IO	Data transmit port 5	Always available
AUD5_TXFS	P1-64*	IO	Frame sync transmit port 5	Always available
	P1-97*			Always available
AUDMUX port 6				
AUD6_RXC	P1-83*	IO	Clock receive port 6	Always available
AUD6_RXD	P1-60*	IO	Data receive port 6	Always available
AUD6_RXFS	P1-82*	IO	Frame sync receive port 6	Always available
AUD6_TXC	P1-105*	IO	Clock transmit port 6	Always available
AUD6_TXD	P1-109*	IO	Data transmit port 6	Always available
AUD6_TXFS	P1-107*	IO	Frame sync transmit port 6	Always available

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.5 of this document.

4.5 High-Definition Multimedia Interface (HDMI)

The HDMI interface available with CM-FX6 is based on the "HDMI transmitter" & "HDMI 3D Tx PHY" integrated into the i.MX6 SoC. The "HDMI transmitter" combines video/display data from the IPU, Audio data from i.MX6 memory & control/status data from the ARM complex, into TMDS data & clock channels. The "HDMI 3D Tx PHY" transmits the combined data by means of 3 TMDS data pairs and a TMDS clock pair to the CM-FX6 carrier board interface.

Figure 3 shows the video/display data path from the IPU to the CM-FX6 carrier board interface through the HDMI transmitter & PHY. The HDMI audio data path is shown in Figure 4.

The HDMI 3D Tx PHY integrated into the i.MX6 SoC supports the following standards & features:

- High-Definition Multimedia Interface Specification, Version 1.4a
- Digital Visual Interface, Revision 1.0
- HDMI Compliance Test Specification, Version 1.4a
- Support for up to 720p at 100Hz and 720i at 200Hz or 1080p at 60Hz and 1080i/720i at 120Hz HDTV display resolutions and up to QXGA graphic display resolutions.
- Support for 4k x 2k and 3D video formats
- Support for up to 16-bit Deep Color modes

Table 19 summarizes the HDMI signals available with CM-FX6. For additional details, please refer to chapters 32 and 33 of the "i.MX6 Reference Manual".

Table 19 HDMI signals

Signal Name	Pin #	Type	Description	Availability
HDMI_TMDS_CLK_DN	P2-16	AO	TMDS clock pair	Always available
HDMI_TMDS_CLK_DP	P2-18	AO		Always available
HDMI_TMDS_DATA0_DN	P2-22	AO	TMDS data 0 pair	Always available
HDMI_TMDS_DATA0_DP	P2-24	AO		Always available
HDMI_TMDS_DATA1_DN	P2-42	AO	TMDS data 1 pair	Always available
HDMI_TMDS_DATA1_DP	P2-44	AO		Always available
HDMI_TMDS_DATA2_DN	P2-48	AO	TMDS data 2 pair	Always available
HDMI_TMDS_DATA2_DP	P2-50	AO		Always available
HDMI_CEC	P2-6*	IO	Consumer Electronics Control signal	Always available
HDMI_HPD	P2-32	I	Hot Plug Detect signal, 5V tolerant.	Always available
DDC_SCL	P1-116*	IO	VESA Data Display Channel clock signal	Always available
DDC_SDA	P1-125*	IO	VESA Data Display Channel data signal	Always available

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.5 of this document.

4.6 WLAN and Bluetooth

CM-FX6 features 802.11b/g/n and Bluetooth 3.0 + HS wireless connectivity solution, implemented with the AzureWave AW-NH387 WLAN + Bluetooth combo controller module. The AW-NH387 is based on the Marvell 88W8787 chipset.

WLAN Standards supported:

- 802.11b: 1, 2, 5.5, 11Mbps
- 802.11g: 6, 9, 12, 18, 24, 36, 48, 54Mbps
- 802.11n up to 150Mbps

WLAN Security features:

- WAPI
- WEP 64-bit and 128-bit encryption with H/W TKIP processing
- WPA/WPA2 (Wi-Fi Protected Access)
- AES-CCMP hardware implementation as part of 802.11i security standard

Bluetooth standards supported:

- Bluetooth 2.1+EDR data rates of 1, 2 and 3 Mbps

Co-Existence:

- Bluetooth and cell phone(GSM/DCS/WCDMA/UMTS/3G) co-existence

The AW-NH387 module communicates with i.MX6 SoC through AUDMUX port 3 and SDIO port 1 of the i.MX6 SoC.

Antenna Connection

The AW-NH387 requires a single 2.4GHz antenna for WIFI & Bluetooth. The antenna is connected via the on-board UFL high frequency connector J1. Any type of 2.4GHz antenna can be used. Please refer to section 6.3 for connector location.

Table 20 J1 connector data

Manufacturer	Mfg. P/N	Mating Connector
Hirose	U.FL-R-MT(10)	Hirose U.FL-LP-040

Table 21 802.11b/g (WLAN) RF system specifications

Feature	Description
Frequency Band	2.4 GHz ISM radio band
Number of Channels	802.11b: USA, Canada and Taiwan – 11 Most European Countries – 13 France – 4, Japan – 14 802.11g: USA, Canada and Taiwan – 11 Most European Countries – 13 Japan – 13 802.11n(HT20): Channel 1~13(2412~2472) 802.11n(HT40): Channel 3~11(2422~2462)
Modulation	DSSS, OFDM, DBPSK, DQPSK, CCK, 16-QAM, 64-QAM for WLAN GFSK (1Mbps), II/4 DQPSK (2Mbps) and 8DPSK (3Mbps) for Bluetooth
Medium Access Protocol	CSMA/CA with ACK
Receive Sensitivity	WLAN:

Feature	Description
	802.11b: Minimum -86+-2dBm at 11Mbps 802.11g: Minimum -71+-2dBm at 54Mbps 802.11n: Minimum -68+-2dBm at HT20 MCS7 Minimum -65+-2dBm at HT40 MCS7 Bluetooth: GFSK: typical -87dBm ΠΙ/4 DQPSK: typical -88dBm 8DPSK: typical -81dBm
Output Power	WLAN: 802.11b(Ch1~13): typical 17dBm +/- 2dBm 802.11b(Ch14): typical 10dBm +/- 2dBm 802.11g: typical 14dBm +/- 2dBm 802.11n: typical HT20 13dBm +/- 2dBm HT40 12dBm +/- 2dBm Bluetooth Bluetooth Class 1.5>1dBm

For additional details, please refer to the AzureWave AW-NH387 datasheet.

NOTE: The WLAN and Bluetooth module is available only with the 'WB' configuration option.

4.7 MediaLB device interface

The Media Local Bus (MediaLB) is a standardized, inter-chip communication bus for "MOST" based devices. CM-FX6 can act as a MediaLB device, utilizing the i.MX6 integrated MLB150 block which implements all the required functionality, including:

- Transmission of commands and data when functioning as the transmitting device associated with a channel address
- Reception of data and transmission of Rx status responses when functioning as the receiving device associated with a channel address
- MediaLB lock detection
- SystemChannel command handling

The MediaLB interface is accessible through the carrier board interface either as a differential interface (6pins) or as a single ended interface (3 pins). The MediaLB audio path is illustrated in Figure 4.

Table 22 summarizes the MLB signals available with CM-FX6. For additional details, please refer to chapter 42 of the "i.MX6 Reference Manual".

Table 22 MediaLB signals

Signal Name	Pin #	Type	Description	Availability
Differential Interface				
MLB_CP	P2-1	AI	Differential MediaLB bus clock	Please contact CompuLab
MLB_CN	P2-3			
MLB_SP	P2-10	AIO	Differential MediaLB signaling information	Please contact CompuLab
MLB_SN	P2-12			
MLB_DP	P2-2	AIO	Differential MediaLB data	Please contact CompuLab
MLB_DN	P2-4			
Single Ended Interface				
MLBCLK	P2-39*	I	Single ended MediaLB bus clock	Please contact CompuLab
MLBSIG	P2-20*	IO	Single ended MediaLB signaling information	Please contact CompuLab
MLBDAT	P1-58*	IO	Single ended MediaLB data	Please contact CompuLab

NOTE: The MediaLB device controller in not available by default. Please contact CompuLab for more information.

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.5 of this document.

NOTE: The MediaLB device controller must use a single interface type, either the differential interface or the single ended interface.

4.8 Ethernet

CM-FX6 incorporates a full-featured 10/100/1000 Ethernet interface, implemented with the i.MX6 integrated Ethernet MAC (ENET) coupled with the AR8033 RGMII Ethernet PHY from Atheros.

The CM-FX6 Ethernet interface supports the following main features:

- 10/100/1000 BASE-T IEEE 802.3 compliant
- IEEE 802.3u compliant Auto-Negotiation
- Integrated IEEE 1588 time stamping module (inside the MAC).
- Automatic channel swap (ACS)
- Full- and Half-duplex
- Automatic MDI/MDIX crossover
- Automatic polarity correction
- Activity and speed indicator LED controls

Table 23 summarizes the Ethernet signals accessible through the CM-FX6 carrier board interface. For additional details, please refer to chapter 42 of the "i.MX6 Reference Manual".

Table 23 Ethernet interface signals

Signal Name	Pin #	Type	Description	Availability
ETH_MDI0P	P1-2	AIO	Media-dependent interface 0, differential 100Ω transmission line	Only available **with** 'E' option.
ETH_MDI0N	P1-4	AIO		Only available **with** 'E' option.
ETH_MDI1P	P1-1	AIO	Media-dependent interface 1, differential 100Ω transmission line	Only available **with** 'E' option.
ETH_MDI1N	P1-3	AIO		Only available **with** 'E' option.
ETH_MDI2P	P1-10	AIO	Media-dependent interface 2, differential 100Ω transmission line	Only available **with** 'E' option.
ETH_MDI2N	P1-12	AIO		Only available **with** 'E' option.
ETH_MDI3P	P1-9	AIO	Media-dependent interface 3, differential 100Ω transmission line	Only available **with** 'E' option.
ETH_MDI3N	P1-11	AIO		Only available **with** 'E' option.
ETH_LED1	P1-6	IO^	Active High, activity LED driver	Only available **with** 'E' option.
ETH_LED2	P1-5	IO^	Active High, 10/100 link LED driver	Only available **with** 'E' option.
ETH_LED3	P1-13	IO^	Active High, 1Gbps link LED driver	Only available **with** 'E' option.

NOTE: For magnetics selection recommendations, please refer to section 8.3 of this document.

NOTE: Signal denoted with ^ are fixed 2.5V logic. These pins must not be driven by the carrier board during CM-FX6 boot process.

4.9 USB 2.0

4.9.1 USB 2.0 On-The-Go

The USB 2.0 OTG interface is implemented with the i.MX6 USB 2.0 OTG controller. The interface provides the following features:

- Supports USB 2.0 High Speed (480Mbps), Full Speed (12Mbps) and Low Speed (1.5Mbps) operation in host mode
- Supports USB 2.0 High Speed (480 Mbps) and Full Speed (12 Mbps) operation in peripheral mode.
- Hardware support for OTG signaling, session request protocol, and host negotiation protocol
- Up to 8 bidirectional endpoints

Table 24 USB 2.0 OTG interface signals

Signal Name	Pin #	Type	Description	Availability
USBOTG_DP	P2-132	AIO	USB OTG positive data	Always available
USBOTG_DN	P2-130	AIO	USB OTG negative data	Always available
USBOTG_ID	P2-128*	AIO	USB OTG ID signal	Always available
	P2-71*			Always available
USBOTG_VBUS	P2-116	P	CM-FX6 does not supply VBUS power. This pin must be connected to the 5V VBUS rail. VBUS can either be supplied by an external system or generated on-board the carrier board. CM-FX6 can draw up to 50mA from this pin	Always available
USBOTG_OC	P2-27*	I	Active low input, designed to inform CM-FX6 of an overcurrent condition on USBOTG_VBUS rail (if detected by the VBUS power supply). Low = Overcurrent detected.	Always available
	P2-85*			Always available
USBOTG_CPEN	P2-104*	O	Active high output, driven by CM-FX6 to enable/disable the USBOTG_VBUS power supply. High = VBUS enabled.	Always available
	P2-87*			Always available
USBOTG_nCHD	P1-80	OD	Active low charger detection output. This signal can be used by the system to indicate that a battery charger is connected to the OTG port.	Always available

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.5 of this document.

4.9.2 USB 2.0 Host

The CM-FX6 high-speed USB interface is implemented with the i.MX6 high-speed USB host port 1. The interface supports the following features:

- Supports USB 2.0 High Speed (480Mbps), Full Speed (12Mbps) and Low Speed (1.5Mbps) operation
- Complies with EHCI (high-speed host controller)

CM-FX6 enables up to 4 USB Host ports by utilizing an optional on-board USB2.0 hub. The USB2.0 host ports mapping is shown in Figure 5.

Figure 5 USB2.0 Host ports

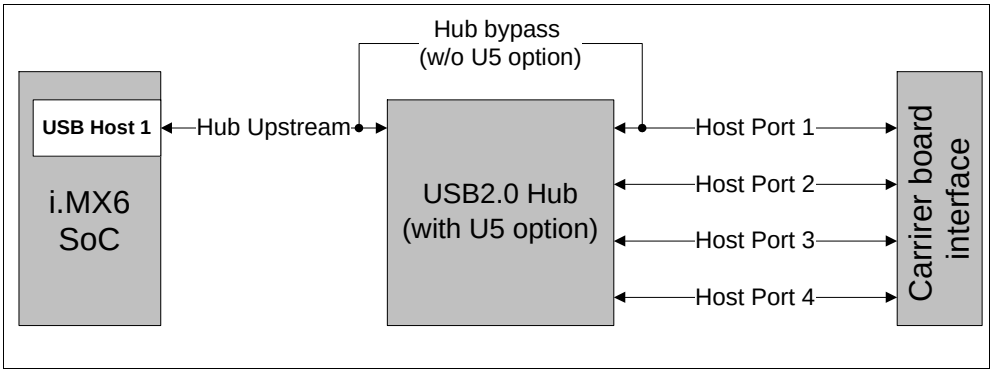


Table 25 USB 2.0 Host interface signals

Signal Name	Pin #	Type	Description	Availability
Host Port-1				
USB1_DP	P1-132	AIO	USB host port 1 positive data	Always available
USB1_DN	P1-130	AIO	USB host port 1 negative data	Always available
USB1_CPEN	P1-124*	O	Active high output, driven by CM-FX6 to enable/disable the USB1_VBUS power supply. High = VBUS enabled.	Always available **NOTE:** This pin may be used for other interfaces as described in chapter 5.5**,** only in case CM-FX6 is assembled **without** the 'U5' option.
	P1-44*			Only available **without** 'U5' option
USB1_VBUS	P1-140	P	CM-FX6 does not supply VBUS power. In case CM-FX6 is assembled without the 'U5' option, this pin must be connected to the 5V VBUS rail. The VBUS rail can be generated on-board the carrier board (See SB-FX6 schematics). CM-FX6 can draw up to 50mA from this pin. In case CM-FX6 is assembled with the 'U5' option, this pin can be left floating.	Only available **without** 'U5' option
USB1_nOVC	P1-46*	I	Active low input, designed to inform CM-FX6 of an overcurrent condition on USB1_VBUS rail (if detected by the VBUS power supply). Low = Overcurrent detected.	Only available **without** 'U5' option
	P1-106	PU33		Only available **with** 'U5' option
Host Port-2				
USB2_DP	P1-138	AIO	USB host port 2 positive data	Only available **with** 'U5' option
USB2_DN	P1-136	AIO	USB host port 2 negative data	Only available **with** 'U5' option

Signal Name	Pin #	Type	Description	Availability
USB2_CPEN	P1-128	O	Active high output, driven by CM-FX6 to enable/disable the VBUS power supply for USB Host port 2. High = VBUS enabled.	Only available **with** 'U5' option
USB2_nOVC	P2-140	PU33	Active low input, designed to inform CM-FX6 of an overcurrent condition on VBUS rail of USB Host port 2 (if detected by the VBUS power supply). Low = Overcurrent detected.	Only available **with** 'U5' option
Host Port-3				
USB3_DP	P1-131	AIO	USB host port 2 positive data	Only available **with** 'U5' option
USB3_DN	P1-129	AIO	USB host port 2 negative data	Only available **with** 'U5' option
USB3_CPEN	P1-126	O	Active high output, driven by CM-FX6 to enable/disable the VBUS power supply for USB Host port 3. High = VBUS enabled.	Only available **with** 'U5' option
USB3_nOVC	P2-138	PU33	Active low input, designed to inform CM-FX6 of an overcurrent condition on VBUS rail of USB Host port 2 (if detected by the VBUS power supply). Low = Overcurrent detected.	Only available **with** 'U5' option
Host Port-4				
USB4_DP	P1-137	AIO	USB host port 2 positive data	Only available **with** 'U5' option
USB4_DN	P1-135	AIO	USB host port 2 negative data	Only available **with** 'U5' option
USB4_CPEN	P1-133	O	Active high output, driven by CM-FX6 to enable/disable the VBUS power supply for USB Host port 4. High = VBUS enabled.	Only available **with** 'U5' option
USB4_nOVC	P2-136	PU33	Active low input, designed to inform CM-FX6 of an overcurrent condition on VBUS rail of USB Host port 2 (if detected by the VBUS power supply). Low = Overcurrent detected.	Only available **with** 'U5' option

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.5 of this document.

4.10 UARTs

Up to 5 UART ports are available with CM-FX6. All the UART ports are derived from the i.MX6 SoC integrated UARTs and support the following features:

- High-speed TIA/EIA-232-F compatible, up to 5.0 Mbit/s.
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s).
- 9-bit or Multidrop mode (RS-485) support (automatic slave address detection).
- 7 or 8 data bits for RS-232 characters or 9 bit RS-485 format, 1 or 2 stop bits.
- Programmable parity (even, odd, and no parity).
- Hardware flow control support for request to send (RTS) and clear to send (CTS) signals
- RXD input and TXD output can be inverted respectively in RS-232/RS-485 mode
- RS-485 driver direction control via CTS signal
- Auto baud rate detection (up to 115.2 Kbit/s)
- Two independent, 32-entry FIFOs for transmit and receive

For additional details, please refer to chapter 62 of the “i.MX6 Reference Manual”.

Table 26 summarizes the UART signals accessible through the CM-FX6 carrier board interface

NOTE: Using UART-4 signals precludes the use of RS-232 port.

Table 26 UART signals

Signal Name	Pin #	Type	Description	Availability
UART-1				
UART1_TX	P1-114*	IO	UART-1 serial / infrared data transmit	Always available
	P1-39*			Only available **without** 'WB' option
UART1_RX	P1-112*	IO	UART-1 serial / infrared data receive	Always available
	P1-41*			Only available **without** 'WB' option
UART1_CTS	P2-54*	IO	UART-1 clear to send.	Always available
UART1_RTS	P2-56*	IO	UART-1 request to send.	Always available
UART1_DSR	P1-73*	I/O	UART-1 Data set ready.	Always available
UART1_DTR	P1-65*	I/O	UART-1 Data terminal ready.	Always available
UART-2				
UART2_TX	P1-42*	IO	UART-2 serial / infrared data transmit	Always available
	P1-72*			Always available
	P2-41*			Always available
UART2_RX	P1-40*	IO	UART-2 serial / infrared data receive	Always available
	P1-61*			Always available
	P2-13*			Always available
UART2_CTS	P1-70*	IO	UART-2 clear to send.	Always available
	P2-25*			Always available
	P2-78*			Always available
UART2_RTS	P1-68*	IO	UART-2 request to send	Always available
	P2-76*			Always available
UART-3				
UART3_TX	P1-65*	IO	UART-3 serial / infrared data transmit	Always available
UART3_RX	P1-73*	IO	UART-3 serial / infrared data receive	Always available
UART3_CTS	P1-46*	IO	UART-3 clear to send.	Always available
	P2-60*			Always available

Signal Name	Pin #	Type	Description	Availability
UART3_RTS	P1-44*	IO	UART-3 request to send.	Always available
UART-4**				
UART4_TX	P2-64*	IO	UART-4 serial / infrared data transmit	Always available
UART4_RX	P2-66*	IO	UART-4 serial / infrared data receive	Always available
UART4_CTS	P2-80*	IO	UART-4 clear to send.	Always available
UART4_RTS	P2-72*	IO	UART-4 request to send.	Always available
UART-5				
UART5_TX	P1-64*	IO	UART-5 serial / infrared data transmit	Always available
	P2-68*			Always available
UART5_RX	P1-66*	IO	UART-5 serial / infrared data receive	Always available
	P2-70*			Always available
UART5_CTS	P2-84*	IO	UART-5 clear to send.	Always available
	P2-87*			Always available
UART5_RTS	P2-82*	IO	UART-5 request to send.	Always available
	P2-85*			Always available

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.5 of this document.

NOTE: Direction of RX, TX, CTS, and RTS signals depends on UART controller configuration (by software).

4.11 RS232

The CM-FX6 incorporates a single RS232 port. The following features are supported:

- 32-entry FIFO for receiver and 32-entry FIFO for transmitter
- Programmable baud rate of up to 250 kbit/s
- 7 or 8 data bits per symbol.
- RS-232 bus-pin ESD protection exceeds ±15 kV using the Human-Body Model

The RS232 port is derived from UART-4 of the i.MX6 SoC.

NOTE: The RS232 port operates at RS232 voltage levels.

NOTE: Using the RS-232 port precludes the use of UART-4 port.

Table 27 RS232 signals

Signal Name	Pin #	Type	Description
RS232_TXD	P1-119	O	RS232 serial data out
RS232_RXD	P1-117	I	RS232 serial data in

4.12 MMC / SD / SDIO

The CM-FX6 features 3 MMC / SD / SDIO host interfaces implemented with the i.MX6 integrated "Ultra Secured Digital Host Controller" (uSDHC). The following main features are supported by uSDHC:

- Compatible with the MMC System Specification version 4.2/4.3/4.4/4.5.
- Conforms to the SD Host Controller Standard Specification version 3.0.
- Compatible with the SD Memory Card Specification version 3.0 and supports the "Extended Capacity SD Memory Card".
- Compatible with the SDIO Card Specification version 3.0.
- Supports 1-bit / 4-bit SD and SDIO modes, 1-bit / 4-bit
- 8-bit MMC modes (MMC-3 only).

Each MMC/SD/SDIO host controller can support a single MMC / SD / SDIO card or device.

The MMC-1 controller interface controller interface supports up to 4-bit transfer modes. This interface is used for CM-FX6 WLAN and Bluetooth functionality ("WB" product option). In case the "WB" option is not populated on-board CM-FX6, MMC-1 is accessible through the carrier board interface.

The MMC-2 controller interface supports up to 4-bit transfer modes. This interface is only available at the carrier board interface whenever CM-FX6 does not include the optional analog audio codec ("A" product option).

The MMC-3 controller interface supports up to 8-bit transfer modes. MMC-3 is always accessible through the carrier board interface. The MMC-3 interface is bootable, meaning CM-FX6 can boot from an SD card over the MMC-3 interface.

For additional details, please refer to chapter 65 of the "I.MX6 Reference Manual".

Table 28 MMC / SD / SDIO signals

Signal Name	Pin #	Type	Description	Availability
MMC-1				
MMC1_CLK	P2-73*	IO	Interface clock	Only available **without** 'WB' option
MMC1_CMD	P2-75*	IO	Command signal	Only available **without** 'WB' option
MMC1_DAT0	P2-61*	IO	Card data bit 0	Only available **without** 'WB' option
MMC1_DAT1	P2-63*	IO	Card data bit 1	Only available **without** 'WB' option
MMC1_DAT2	P2-65*	IO	Card data bit 2	Only available **without** 'WB' option
MMC1_DAT3	P2-69*	IO	Card data bit 3	Only available **without** 'WB' option
MMC1_LCTL	P1-20*	O	An external LED control signal, designed to indicate that the SD interface is busy	Always available
MMC1_CD	P2-71*	I	Active low card detection signal	Always available
MMC1_WP	P1-60*	I	Active low write protection signal	Always available
	P2-77*			Always available
MMC-2				
MMC2_CLK	P2-59*	IO	Interface clock	Only available **without** 'A' option
MMC2_CMD	P2-57*	IO	Command signal	Only available **without** 'A' option
MMC2_DAT0	P2-47*	IO	Card data bit 0	Only available **without** 'A' option
MMC2_DAT1	P2-51*	IO	Card data bit 1	Only available **without** 'A' option
MMC2_DAT2	P2-49*	IO	Card data bit 2	Only available **without** 'A' option
MMC2_DAT3	P2-45*	IO	Card data bit 3	Only available **without** 'A' option
MMC2_CD	P1-56*	I	Active low card detection signal	Always available
MMC2_WP	P1-58*	I	Active low write protection signal	Always available
MMC-3				
MMC3_CLK	P2-76*	IO	MMC3 Interface clock	Always available
MMC3_CMD	P2-78*	IO	Command signal	Always available

MMC3_DAT0	P2-54*	IO	Card data bit 0	Always available
MMC3_DAT1	P2-56*	IO	Card data bit 1	Always available
MMC3_DAT2	P2-58*	IO	Card data bit 2	Always available
MMC3_DAT3	P2-60*	IO	Card data bit 3	Always available
MMC3_DAT4	P2-13*	IO	Card data bit 4	Always available
MMC3_DAT5	P2-41*	IO	Card data bit 5	Always available
MMC3_DAT6	P1-112*	IO	Card data bit 6	Always available
MMC3_DAT7	P1-114*	IO	Card data bit 7	Always available

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.5 of this document.

4.13 Touch-Screen

CM-FX6 features an optional on-board resistive touch-screen controller. The controller is communicating with the i.MX6 SoC over the SPI-1 interface. The interface supports 4-wire touch panels and is available through the CM-FX6 carrier board interface.

Table 29 Touch-screen signals

Signal Name	Pin #	Type	Description	Availability
TS_X+	P1-23	AIO	Touch screen X+ (right)	Only available **with** 'I' option.
TS_X-	P1-21	AIO	Touch screen X- (left)	Only available **with** 'I' option.
TS_Y+	P1-29	AIO	Touch screen Y+ (top)	Only available **with** 'I' option.
TS_Y-	P1-27	AIO	Touch screen Y- (bottom)	Only available **with** 'I' option.

4.14 Keypad

The CM-FX6 CoM features a 7x7 matrix keypad interface derived from the keypad port (KPP) included with the i.MX6 SoC. The KPP supports the following features:

- Open drain design
- Glitch suppression circuit design
- Multiple-key detection
- Long key-press detection
- Supports a 2-point and 3-point contact key matrix

For additional details, please refer to chapter 37 of the "I.MX6 Reference Manual".

Table 30 Keypad signals

Signal Name	Pin #	Type	Description	Availability
KPD_ROW1	P1-66*	SPU	Row 1	Always available
KPD_ROW2	P2-6*	SPU	Row 2	Always available
KPD_ROW3	P1-125*	SPU	Row 3	Always available
KPD_ROW4	P2-87*	SPU	Row 4	Always available
KPD_ROW5	P1-45*	SPU	Row 5	Only available **without** 'WB' option
	P2-57*	SPU		Only available **without** 'A' option
	P2-71*	SPU		Always available
KPD_ROW6	P1-49*	SPU	Row 6	Only available **without** 'WB' option
	P1-58*	SPU		Always available
	P2-49*	SPU		Only available **without** 'A' option
KPD_ROW7	P1-35*	SPU	Row 7	Always available
	P2-47*	SPU		Only available **without** 'A' option
	P2-53*	SPU		Only available **without** 'A' option
KPD_COL1	P1-64*	OD	Column 1	Always available
KPD_COL2	P2-5*	OD	Column 2	Always available
KPD_COL3	P1-116*	OD	Column 3	Always available
KPD_COL4	P2-85*	OD	Column 4	Always available
KPD_COL5	P1-124*	OD	Column 5	Only available **without** 'U5' option
	P1-32*	OD		Always available
	P1-48*	OD		Only available **without** 'WB' option
	P2-59*	OD		Only available **without** 'A' option
KPD_COL6	P1-47*	OD	Column 6	Only available **without** 'WB' option
	P2-45*	OD		Only available **without** 'A' option
	P2-77*	OD		Always available
KPD_COL7	P1-56*	OD	Column 7	Always available
	P1-33*	OD		Always available
	P2-51*	OD		Only available **without** 'A' option

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.5 of this document.

4.15 GPIO

CM-FX6 provides up to 112 GPIO signals. The GPIO subsystem is derived from the i.MX6 integrated GPIO controller. i.MX6 GPIOs are divided into 8 blocks with up to 32 GPIOs in each block (a total of 8 x 32 = 256 GPIOs). The GPIO signals can be configured for the following applications:

- Data input / output
- Interrupt generation

For additional details, please refer to section 27 of the "I.MX6 Reference Manual".

NOTE: Not all GPIO signals supported by the i.MX6 SoC are available through the CM-FX6 carrier board interface.

Table 31 GPIO availability

Signal name	Pin #	Type	Availability
GPIO1_0	P1-124*	IO	Only available **without** 'U5' option
GPIO1_1	P2-71*	IO	Always available
GPIO1_2	P1-58*	IO	Always available
GPIO1_4	P1-56*	IO	Always available
GPIO1_5	P2-53*	IO	Only available **without** 'A' option
GPIO1_7	P1-72*	IO	Always available
GPIO1_8	P1-61*	IO	Always available
GPIO1_9	P2-77*	IO	Always available
GPIO1_10	P2-59*	IO	Only available **without** 'A' option
GPIO1_11	P2-57*	IO	Only available **without** 'A' option
GPIO1_12	P2-45*	IO	Only available **without** 'A' option
GPIO1_13	P2-49*	IO	Only available **without** 'A' option
GPIO1_14	P2-51*	IO	Only available **without** 'A' option
GPIO1_15	P2-47*	IO	Only available **without** 'A' option
GPIO1_16	P2-61*	IO	Only available **without** 'WB' option
GPIO1_17	P2-63*	IO	Only available **without** 'WB' option
GPIO1_18	P2-75*	IO	Only available **without** 'WB' option
GPIO1_19	P2-65*	IO	Only available **without** 'WB' option
GPIO1_20	P2-73*	IO	Only available **without** 'WB' option
GPIO1_21	P2-69*	IO	Only available **without** 'WB' option
GPIO1_24	P2-128*	IO	Always available
GPIO1_25	P2-89*	IO	Always available
GPIO1_26	P2-20*	IO	Always available
GPIO1_27	P2-121*	IO	Always available
GPIO1_29	P2-39*	IO	Always available
GPIO2_9	P2-40*	IO	Always available
GPIO2_10	P2-29*	IO	Always available
GPIO2_13	P1-68*	IO	Always available
GPIO2_14	P1-70*	IO	Always available
GPIO2_23	P1-71*	IO	Always available
GPIO2_24	P1-69*	IO	Always available
GPIO2_25	P1-63*	IO	Always available
GPIO3_21	P2-27*	IO	Always available
GPIO3_22	P2-104*	IO	Always available
GPIO3_24	P1-65*	IO	Always available
GPIO3_25	P1-73*	IO	Always available
GPIO3_26	P1-42*	IO	Always available
GPIO3_27	P1-40*	IO	Always available
GPIO3_28	P2-25*	IO	Always available
GPIO3_30	P1-46*	IO	Always available
GPIO3_31	P1-44*	IO	Always available
GPIO4_5	P1-32*	IO	Always available
GPIO4_8	P1-64*	IO	Always available
GPIO4_9	P1-66*	IO	Always available
GPIO4_10	P2-5*	IO	Always available
GPIO4_11	P2-6*	IO	Always available

Signal name	Pin #	Type	Availability
GPIO4_12	P1-116*	IO	Always available
GPIO4_13	P1-125*	IO	Always available
GPIO4_14	P2-85*	IO	Always available
GPIO4_15	P2-87*	IO	Always available
GPIO4_16	P1-108*	IO	Always available
GPIO4_17	P1-105*	IO	Always available
GPIO4_18	P1-109*	IO	Always available
GPIO4_19	P1-107*	IO	Always available
GPIO4_20	P1-60*	IO	Always available
GPIO4_21	P1-75*	IO	Always available
GPIO4_22	P1-76*	IO	Always available
GPIO4_23	P1-77*	IO	Always available
GPIO4_24	P1-78*	IO	Always available
GPIO4_25	P1-81*	IO	Always available
GPIO4_26	P1-82*	IO	Always available
GPIO4_27	P1-83*	IO	Always available
GPIO4_28	P1-84*	IO	Always available
GPIO4_29	P1-85*	IO	Always available
GPIO4_30	P1-87*	IO	Always available
GPIO4_31	P1-88*	IO	Always available
GPIO5_5	P1-89*	IO	Always available
GPIO5_6	P1-90*	IO	Always available
GPIO5_7	P1-92*	IO	Always available
GPIO5_8	P1-93*	IO	Always available
GPIO5_9	P1-94*	IO	Always available
GPIO5_10	P1-95*	IO	Always available
GPIO5_11	P1-96*	IO	Always available
GPIO5_12	P1-97*	IO	Always available
GPIO5_13	P1-99*	IO	Always available
GPIO5_14	P1-100*	IO	Always available
GPIO5_15	P1-101*	IO	Always available
GPIO5_16	P1-102*	IO	Always available
GPIO5_17	P1-104*	IO	Always available
GPIO5_18	P1-57*	IO	Always available
GPIO5_19	P1-51*	IO	Always available
GPIO5_20	P1-59*	IO	Always available
GPIO5_21	P1-53*	IO	Always available
GPIO5_22	P1-48*	IO	Only available **without** 'WB' option
GPIO5_23	P1-45*	IO	Only available **without** 'WB' option
GPIO5_24	P1-47*	IO	Only available **without** 'WB' option
GPIO5_25	P1-49*	IO	Only available **without** 'WB' option
GPIO5_26	P1-33*	IO	Always available
GPIO5_27	P1-35*	IO	Always available
GPIO5_28	P1-39*	IO	Only available **without** 'WB' option
GPIO5_29	P1-41*	IO	Only available **without** 'WB' option
GPIO5_30	P2-64*	IO	Always available
GPIO5_31	P2-66*	IO	Always available
GPIO6_0	P2-68*	IO	Always available
GPIO6_1	P2-70*	IO	Always available
GPIO6_2	P2-72*	IO	Always available
GPIO6_3	P2-80*	IO	Always available
GPIO6_4	P2-82*	IO	Always available
GPIO6_5	P2-84*	IO	Always available
GPIO6_15	P2-97*	IO	Always available
GPIO6_17	P1-114*	IO	Always available
GPIO6_18	P1-112*	IO	Always available
GPIO7_0	P2-41*	IO	Always available
GPIO7_1	P2-13*	IO	Always available
GPIO7_11	P1-20*	IO	Always available
GPIO7_13	P2-119*	IO	Always available
GPIO7_2	P2-78*	IO	Always available
GPIO7_3	P2-76*	IO	Always available
GPIO7_4	P2-54*	IO	Always available
GPIO7_5	P2-56*	IO	Always available
GPIO7_6	P2-58*	IO	Always available
GPIO7_7	P2-60*	IO	Always available

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.5 of this document.

4.16 I²C

The CM-FX6 features three general purpose I²C interfaces. The following features are supported:

- Compliance with Philips I²C specification version 2.1
- Multiple-master operation
- Support for standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s)
- Arbitration-lost interrupt with automatic mode switching from master to slave

The I²C interfaces are implemented with the i.MX6 integrated I²C controller. For additional details, please refer to section 34 of the "I.MX6 Reference Manual".

Table 32 I²C signals

Signal Name	Pin #	Type	Description	Availability
I²C-1				
I2C1_SDA	P1-33*	IO	I²C serial data line	Always available
	P2-25*	IO		Always available
I2C1_SCL	P1-35*	IO	I²C serial clock line	Always available
	P2-27*	IO		Always available
I²C-2				
I2C2_SDA	P1-125*	IO	I²C serial data line	Always available
I2C2_SCL	P1-116*	IO	I²C serial clock line	Always available
I²C-3**				
I2C3_SDA	P1-20*	IO	I²C serial data line	Only available **without** 'A' option. Prevents access to on-board E²PROM
I2C3_SCL	P2-53*	IO	I²C serial clock line	Only available **without** 'A' option. Prevents access to on-board E²PROM

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.5 of this document.

NOTE: The CM-FX6 on-board EEPROM is interfaced with the i.MX6 SoC through the I²C-3 interface. Utilizing I²C-3 at the carrier board prevents i.MX6 SoC from accessing the CM-FX6 on-board EEPROM.

4.17 SPI

CM-FX6 features five Enhanced Configurable SPI ports. All CM-FX6 SPI ports are derived from the i.MX6 SoC integrated ECSPI IPs. The following main features are supported:

- Full-duplex synchronous serial interface
- Master/Slave configurable
- Transfer continuation function allows unlimited length data transfers
- 32-bit wide by 64-entry FIFO for both transmit and receive data
- 32-bit wide by 16-entry FIFO for HT message data
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable Direct Memory Access (DMA) support

For additional details, please refer to section 20 of the "I.MX6 Reference Manual".

Table 33 SPI signals

Signal Name	Pin #	Type	Description	Availability
SPI-1**				
SPI1_CLK	P1-100*	IO	SPI-1 clock	Only available **without** 'I' option.
	P1-48*			Only available **without** 'I' option. Only available **without** 'WB' option.
SPI1_CS0	P1-104*	IO	SPI-1 Chip select 0	Always available
	P1-49*			Only available **without** 'WB' option.
	P1-66*			Always available
SPI1_CS1	P1-94*	IO	SPI-1 Chip select 1	Only available **without** 'I' option.
	P2-5*			Only available **without** 'I' option.
SPI1_CS2	P1-65*	IO	SPI-1 Chip select 2	Always available
	P2-6*			Always available
SPI1_CS3	P1-116*	IO	SPI-1 Chip select 3	Always available
	P1-73*			Always available
SPI1_MOSI	P1-101*	IO	SPI-1 Master data out; slave data in	Only available **without** 'I' option.
	P1-45*			Only available **without** 'I' option. Only available **without** 'WB' option.
SPI1_MISO	P1-102*	IO	SPI-1 Master data in; slave data out	Only available **without** 'I' option.
	P1-47*			Only available **without** 'I' option. Only available **without** 'WB' option.
	P1-64*			Only available **without** 'I' option.
SPI1_RDY	P1-32*	I	SPI-1 optional data ready signal	Always available
SPI-2				
SPI2_CLK	P1-33*	IO	SPI-2 clock	Always available
	P1-71*			Always available
	P1-99*			Always available
SPI2_CS0	P1-41*	IO	SPI-2 Chip select 0	Only available **without** 'WB' option.
	P1-97*			Always available
SPI2_CS1	P1-94*	IO	SPI-2 Chip select 1	Always available
SPI2_CS2	P1-65*	IO	SPI-2 Chip select 2	Always available
SPI2_CS3	P1-73*	IO	SPI-2 Chip select 3	Always available
SPI2_MOSI	P1-35*	IO	SPI-2 Master data out; slave data in	Always available
	P1-69*			Always available
	P1-95*			Always available
SPI2_MISO	P1-39*	IO	SPI-2 Master data in; slave data out	Only available **without** 'WB' option.
	P1-63*			Always available
	P1-96*			Always available
SPI-3				
SPI3_CLK	P1-75*	IO	SPI-3 clock	Always available
SPI3_CS0	P1-78*	IO	SPI-3 Chip select 0	Always available
SPI3_CS1	P1-81*	IO	SPI-3 Chip select 1	Always available
SPI3_CS2	P1-82*	IO	SPI-3 Chip select 2	Always available
SPI3_CS3	P1-83*	IO	SPI-3 Chip select 3	Always available

Signal Name	Pin #	Type	Description	Availability
SPI3_MOSI	P1-76*	IO	SPI-3 Master data out; slave data in	Always available
SPI3_MISO	P1-77*	IO	SPI-3 Master data in; slave data out	Always available
SPI3_RDY	P1-84*	I	SPI-3 optional data ready signal	Always available
SPI-4				
SPI4_CLK	P2-27*	IO	SPI-4 clock	Always available
SPI4_CS2	P1-65*	IO	SPI-4 Chip select 2	Always available
SPI4_CS3	P1-73*	IO	SPI-4 Chip select 3	Always available
SPI4_MOSI	P2-25*	IO	SPI-4 Master data out; slave data in	Always available
SPI4_MISO	P2-104*	IO	SPI-4 Master data in; slave data out	Always available
SPI-5				
SPI5_CLK	P2-59*	IO	SPI-5 clock	Only available **without** 'A' option. Only available **with** 'C1200QM' or "C1000DM" option.
	P2-73*			Only available **without** 'WB' option. Only available **with** 'C1200QM' or "C1000DM" options.
SPI5_CS0	P2-51*	IO	SPI-5 Chip select 0	Only available **without** 'A' option. Only available **with** 'C1200QM' or "C1000DM" options.
	P2-63*			Only available **without** 'WB' option. Only available **with** 'C1200QM' or "C1000DM" options.
SPI5_CS1	P2-49*	IO	SPI-5 Chip select 1	Only available **without** 'A' option. Only available **with** 'C1200QM' or "C1000DM" options.
	P2-65*			Only available **without** 'WB' option. Only available **with** 'C1200QM' or "C1000DM" options.
SPI5_CS2	P2-69*	IO	SPI-5 Chip select 2	Only available **without** 'WB' option. Only available **with** 'C1200QM' or "C1000DM" options.
SPI5_CS3	P2-45*	IO	SPI-5 Chip select 3	Only available **without** 'A' option. Only available **with** 'C1200QM' or "C1000DM" options.
SPI5_MOSI	P2-57*	IO	SPI-5 Master data out; slave data in	Only available **without** 'A' option. Only available **with** 'C1200QM' or "C1000DM" options.
	P2-75*			Only available **without** 'WB' option. Only available **with** 'C1200QM' or "C1000DM" options.
SPI5_MISO	P2-47*	IO	SPI-5 Master data in; slave data out	Only available **without** 'A' option. Only available **with** 'C1200QM' or "C1000DM" options.
	P2-61*	IO		Only available **without** 'WB' option. Only available **with** 'C1200QM' or "C1000DM" options.
SPI5_RDY	P1-72*	I	SPI-5 optional data ready signal	Always available

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.5 of this document.

NOTE: The CM-FX6 on-board bootable SPI Flash is interfaced with the i.MX6 SoC through the SPI-1 port on CS0. Utilizing SPI-1 at the carrier board prevents i.MX6 SoC from accessing the on-board SPI Flash during normal operation (CM-FX6 will still access the on-board SPI Flash during the boot process).

4.18 CAN

CM-FX6 features two CAN bus interfaces. The CAN bus interfaces are implemented with the i.MX6 on chip "Flexible Controller Area Network" (FlexCAN) communication modules. FlexCAN supports the following main features:

- Compliant with the CAN 2.0B protocol specification
- Programmable bit rate up to 1 Mb/sec

For additional details, please refer to section 25 of the "I.MX6 Reference Manual".

Table 34 CAN interface signals

Signal Name	Pin #	Type	Description	Availability
CAN-1				
CAN1_TX	P1-72*	O	CAN-1 Transmit serial data pin	Always available
	P2-5*			Always available
	P2-78*			Always available
CAN1_RX	P1-61*	I	CAN-1 Receive serial data pin	Always available
	P2-6*			Always available
	P2-76*			Always available
CAN-2				
CAN2_TX	P2-54*	O	CAN-2 Transmit serial data pin	Always available
	P2-85*			Always available
CAN2_RX	P2-56*	I	CAN-2 Receive serial data pin	Always available
	P2-87*			Always available

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.5 of this document.

4.19 General Purpose Timer (GPT)

CM-FX6 features a general purpose timer (GPT). The GPT is capable of generating an event on CM-FX6 carrier board interface and/or a system interrupt when the timer reaches a programmed value. Additional GPT functionality includes capturing the counter value in a register (this can be triggered by an event on the CM-FX6 carrier board interface). The following main features are supported:

- One 32-bit up-counter with clock source selection, including external clock.
- 12-bit prescaler for division of input clock frequency.
- Two “Capture Event” trigger inputs (2 channels) with a programmable trigger edge.
- Three “Compare Event Occurred” outputs (3 channels) with programmable “active” state. A "forced compare" feature is also available.
- Interrupt generation at capture, compare, and rollover events.
- “Restart” or “free-run” operation modes support.

For additional details, please refer to section 29 of the “i.MX6 Reference Manual”.

Table 35 GPT signals

Signal Name	Pin #	Type	Description	Availability
GPT_CAPIN1	P2-61*	I	“Capture event” trigger input (channel 1)	Only available **without** 'W' option
GPT_CAPIN2	P2-63*	I	“Capture event” trigger input (channel 2)	Only available **without** 'W' option
GPT_CLKIN	P2-73*	I	An optional external counter clock input.	Only available **without** 'W' option
GPT_CMPOUT1	P2-75*	O	“Compare Event Occurred” indicator (channel 1).	Only available **without** 'W' option
GPT_CMPOUT2	P2-65*	O	“Compare Event Occurred” indicator (cchannel 2).	Only available **without** 'W' option
GPT_CMPOUT3	P2-69*	O	“Compare Event Occurred” indicator (cchannel 3).	Only available **without** 'W' option

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.5 of this document.

4.20 Enhanced Periodic Interrupt Timer (EPIT)

CM-FX6 is equipped with two “Enhanced Periodic Interrupt Timers” (EPIT) derived from the i.MX6 SoC capabilities. EPIT is a 32-bit set-and-forget timer that is capable of providing precise interrupts at regular intervals with minimal processor intervention. EPIT has the following key features:

- 32-bit down counter with clock source selection
- 12-bit prescaler for division of input clock frequency
- Interrupt generation when counter reaches the compare value
- A “Compare Event Occurred” output with programmable “active” state.
- “Set-and-Forget” or “free-running” operation modes support.

For additional details, please refer to section 23 of the “i.MX6 Reference Manual”.

Table 36 EPIT signals

Signal Name	Pin #	Type	Description	Availability
EPIT1_OUT	P1-124*	O	“Compare Event Occurred” indicator (EPIT1).	Only available **without** 'U5' option
	P1-72*			Always available
EPIT2_OUT	P1-61*	O	“Compare Event Occurred” indicator (EPIT1).	Always available

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.5 of this document.

4.21 Pulse Width Modulation (PWM)

Four PWM output signals are available at the CM-FX6 carrier board interface. The following key features are supported:

- 16-bit up-counter with clock source selection
- 4 x 16 FIFO to minimize interrupt overhead
- 12-bit prescaler for division of clock
- Active high or active low configured output

For additional details, please refer to section 50 of the “i.MX6 Reference Manual”.

Table 37 PWM signals

Signal Name	Pin #	Type	Description	Availability
PWM1_OUT	P1-85*	O	PWM1 output signal	Always available
	P2-69*			Only available **without** 'W' option
	P2-77*			Always available
PWM2_OUT	P1-87*	O	PWM2 output signal	Always available
	P2-65*			Only available **without** 'W' option
	P2-71*			Always available
PWM3_OUT	P2-40*	O	PWM3 output signal	Always available
	P2-63*			Only available **without** 'W' option
PWM4_OUT	P2-29*	O	PWM4 output signal	Always available
	P2-75*			Only available **without** 'W' option

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.5 of this document.

4.22 Watchdog timers (WDOG)

CM-FX6 is equipped with two "Watchdog timers" (WDOG) derived from the i.MX6 SoC. The WDOG can be used to protect system from failures by providing a method of escaping from unexpected events or programming errors. Once the WDOG is activated, it must be serviced by the software on a periodic basis. If servicing does not take place, the timer times out. Upon a timeout, the WDOG will assert the internal system reset signal. An optional, programmable interrupt can be generated prior to watchdog timer timeout. WDOG supports the following main features:

- A configurable timeout counter with periods from 0.5 seconds up to 128 seconds.
- Time resolution of 0.5 seconds
- Programmable interrupt generation prior to timeout

For additional details, please refer to section 68 of the "i.MX6 Reference Manual".

Table 38 Watchdog timer signals

Signal Name	Pin #	Type	Description	Availability
WDOG-1				
WDOG1	P1-85	O	Active low signal asserted either upon a WDOG1 "timeout event", by SW or upon a WDOG1 "power-down event"	Always available
	P2-65			Only available **without** 'W' option
	P2-77			Always available
WDOG1_RST	P2-65	O	Active low signal asserted either upon a WDOG1 timeout event, or by SW	Only available **without** 'W' option
WDOG-2				
WDOG2	P1-87	O	Active low signal asserted either upon a WDOG1 "timeout event", by SW or upon a WDOG1 "power-down event"	Always available
	P2-71			Only available **without** 'W' option
	P2-69			Always available
WDOG2_RST	P2-69	O	Active low signal asserted either upon a WDOG2 timeout event, or by SW	Only available **without** 'W' option

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.5 of this document.

4.23 JTAG

The CM-FX6 JTAG interface is derived from the i.MX6 SoC integrated SJC module.

The SJC module implements and manages the daisy-chained topology consisting of its' own TAP and those of the SDMA, and the ARM Debug Access Port (DAP). The SJC supports the following main features:

- IEEE P1149.1, 1149.6 (standard JTAG) interface to off-chip test and development equipment
- Debug-related control and status

For additional details, please refer to the SJC chapter of the "I.MX6 Reference Manual".

Table 39 JTAG signals

Signal Name	Pin #	Type	Description	Availability
JTAG_TCK	P2-90	I	Test clock	Always available
JTAG_TDO	P2-94	O	Test data output	Always available
JTAG_TDI	P2-92	I	Test data input	Always available
JTAG_TMS	P2-96	I	Test mode select	Always available
JTAG_nTRST	P2-88	I	Test logic reset	Always available
JTAG_MOD	P1-25	I	SJC Operation mode selector pin.	Always available

5 SYSTEM LOGIC

CM-FX6 allows access to several system logic related signals through the carrier board interface connectors (P1 and P2). Please refer to chapter 4 of this document for signal description notes and legend.

5.1 Power Management

5.1.1 Power Rails

The CM-FX6 supports two power supply options:

- Regulated DC supply (5V Typical).
- Lithium-ion polymer battery

CM-FX6 does not feature an on-board Lithium-ion polymer battery charger. If required, such a charger must be implemented on the carrier board.

Table 40 Power signals

Signal Name	Type	Description
V_ROOT	P	Main power supply. Connect either to a regulated DC supply (5V Typ.) or directly to a Lithium-ion polymer battery.
VCC_RTC	P	RTC back-up battery power input. Connect to a 3V coin-cell lithium battery.
GND	P	Common ground.

NOTE: VCC_RTC must be at a valid voltage level before V_ROOT in order to ensure proper power-up of CM-FX6.

5.1.2 Low Power Mode

To be added in a future revision of this document.

5.2 Reset

The nCOLD_RST signal is the main system reset input. Driving a logic zero for at least 1mS on the nCOLD_RST signal invokes a global reset that affects every module on CM-FX6. For additional details, please refer to the “System Reset Controller” of the “I.MX6 Reference Manual”.

Table 41 Reset signal

Signal Name	Pin #	Type	Description	Availability
nCOLD_RST	P2-33	PU33	Cold reset input. Active low, 100KΩ pull-up typical resistance.	Always available

5.3 Boot Sequence

The CM-FX6 standard boot sequence provides the following boot options:

- Boot from the on-board SPI NOR flash – default boot device.
- Boot from an external SD card using the MMC-3 interface – alternative boot device.

The standard boot sequence is designed for normal system operation with the on-board SPI NOR flash as the boot media. The ALT_BOOT signal allows using an external SD card as the boot device allowing recovery/upgrade of the on-board boot media.

Table 42 Alternative Boot selection signal

Signal Name	Pin #	Type	Description	Availability
ALT_BOOT	P2-117	PD	Alternative boot device selection. Active high input. May be left floating in case the alternative boot sequence is not desirable.	Always available

Table 43 CM-FX6 Boot devices

ALT_BOOT Logic Value	Boot Device
"0"	On-board SPI Flash
"1"	MMC-3 connected SD card

5.4 System and Miscellaneous Signals

5.4.1 External regulator control

CM-FX6 supports carrier board power supply control by means of two dedicated output signals. Both signals are derived from the i.MX6 SoC. The logic that controls both signals draws its power from the VCC_RTC power rail, meaning that this power supply must always be present in order to use the external regulator control features.

The PMIC_STBY_REQ output can be used to signal carrier board power supply that CM-FX6 is in 'standby' or 'OFF' mode. The PMIC_ON_REQ output indicates only 'OFF' mode. Utilizing the external regulator control signals enables carrier board power management functionality.

For additional details, please refer to the "System Reset Controller" chapter of the "i.MX6 Reference Manual".

Table 44 External regulator control signals

Signal Name	Pin #	Type	Description	Availability
PMIC_STBY_REQ	P2-109	O	System standby indicator output. High when system is in 'standby' or 'OFF' mode.	Always available
PMIC_ON_REQ	P2-37	O	System OFF indicator output, Low when system is in the 'OFF' mode.	Always available

NOTE: The external regulator control signals logic is powered on-board CM-FX6 from the VCC_RTC power supply. VCC_RTC must remain valid at all times for proper operation of these signals.

5.4.2 External DMA Requests

CM-FX6 provides two optional external DMA request signals that can be used by external devices to establish direct hardware synchronization with the i.MX6 internal SDMA controller. A logical channel can be configured to respond to an external synchronization request.

For additional details, please refer to the "Smart Direct Memory Access Controller" chapter of the "i.MX6 Reference Manual".

Table 45 System signals

Signal Name	Pin #	Type	Description	Availability
SDMA_EXT_EVT0	P1-92*	I	External DMA request 0	Always available
SDMA_EXT_EVT1	P1-93*	I	External DMA request 1	Always available
	P1-83*			Always available

NOTE: Pins denoted with "*" may be used for other interfaces. For details, please refer to section 5.5 of this document.

5.4.3 General Purpose differential clock I/O

The general purpose clocks available with CM-FX6 are LVDS input/output differential pairs compatible with the TIA/EIA-644 standard and capable of driving an up to 600MHz clock to the system. The signals can also be used as single ended clock inputs into the CM-FX6. Any of the signals can be configured as follows:

- As inputs to feed external reference clocks to the i.MX6 on-chip PLLs and/or modules, for example as alternate reference clock for PCIe or/and SATA or video/audio interfaces.
- As outputs to be used as either a reference clock or as a functional clock for peripherals, for example an output of the PCIe master clock (root complex use).

For additional details, please refer to the "Smart Direct Memory Access Controller" of the "i.MX6 Reference Manual".

Table 46 General Purpose differential clock signals

Signal Name	Pin #	Type	Description	Availability
GENP_LVDSCLK1_DP	P2-101	AIO	Positive side of LVDS clock 1 output. Can also be used as a single ended input	Always available
GENP_LVDSCLK1_DN	P2-99	AIO	Negative side of LVDS clock 1 output. In case GENP_LVDSCLK1_DP is used as input, this signal must be tied to 1.25V. Can	Always available
GENP_LVDSCLK2_DP	P1-54	AIO	Positive side of LVDS clock 2 output. Can also be used as a single ended input	Always available
GENP_LVDSCLK2_DN	P1-52	AIO	Negative side of LVDS clock 2 output. In case GENP_LVDSCLK2_DN is used as input, this signal must be tied to 1.25V.	Always available

5.4.4 Flash Write-protection.

The on-board SPI NOR flash is the default boot-loader storage as described in chapter 3.3.2. The FLASH_nWP signal can be used to prevent accidental corruption of the SPI Flash stored data.

NOTE: The FLASH_nWP must be used in conjunction with SW to enable write protection. Using the FLASH_nWP signal alone will not enable write protection.

Table 47 Flash Write protection signals

Signal Name	Pin #	Type	Description	Availability
FLASH_nWP	P2-46	PU33	Active low input to allow SPI Flash write-protection.	Always available

5.4.5 SSD Activity indicator

The CM-FX6 optional on-board SATA-II SSD is equipped with a 'Device Activity Signal'. The signal can be used to control a LED indicating the on-board SSD activity.

Table 48 External regulator control signals

Signal Name	Pin #	Type	Description	Availability
ONB_SSD_nACT	P2-123	O	SSD Device Activity Signal	Only available **with** 'ND###' options. Only available **without** 'C1000' option.

5.5 Signal Multiplexing Characteristics

112 of the CM-FX6 carrier board interface pins are multifunctional. Multifunctional pins enable extensive functional flexibility of the CM-FX6 CoM by allowing usage of a single carrier board interface pin for one of several functions. Up-to 8 functions (ALT modes) are accessible through each multifunctional carrier board interface pin. The multifunctional capabilities if CM-FX6 pins are derived from the i.MX6 SoC pin mux controller (IOMUX).

NOTE: Pin function selection is controlled by software.

NOTE: Each pin can be used for a single function at a time.

NOTE: Only one pin can be used for each function (in case a function is available on more than one carrier board interface pin).

NOTE: An empty ALT mode must be considered as a "RESERVED" function and must not be used.

Table 49 summarizes the Multifunctional signals available with CM-FX6. For additional details, please refer to the "IOMUX Controller" and "External Signals and Pin Multiplexing" chapters of the i.MX6 Reference Manual.

Table 49 Multifunctional Signals

Pin #	i.MX6 PAD	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
P1-20	GPIO_16	ESAI_TX3_RX2			MMC1_LCTL	SPDIF_IN	GPIO7_11	I2C3_SDA	
P1-32	GPIO_19	KPD_COL5		SPDIF_OUT		SPI1_RDY	GPIO4_5		
P1-33	CSI0_DAT8	IPU0_CSI0_D[8]		SPI2_CLK	KPD_COL7	I2C1_SDA	GPIO5_26		
P1-35	CSI0_DAT9	IPU0_CSI0_D[9]		SPI2_MOSI	KPD_ROW7	I2C1_SCL	GPIO5_27		
P1-39	CSI0_DAT10	IPU0_CSI0_D[10]	AUD3_RXC	SPI2_MISO	UART1_TX		GPIO5_28		
P1-40	EIM_D27			IPU0_CSI0_D[0]		UART2_RX	GPIO3_27		
P1-41	CSI0_DAT11	IPU0_CSI0_D[11]	AUD3_RXFS	SPI2_CS0	UART1_RX		GPIO5_29		
P1-42	EIM_D26			IPU0_CSI0_D[1]		UART2_TX	GPIO3_26		
P1-44	EIM_D31				IPU0_CSI0_D[2]	UART3_RTS	GPIO3_31	USB1_CPEN	
P1-45	CSI0_DAT5	IPU0_CSI0_D[5]		SPI1_MOSI	KPD_ROW5	AUD3_TXD	GPIO5_23		
P1-46	EIM_D30				IPU0_CSI0_D[3]	UART3_CTS	GPIO3_30	USB1_nOVC	
P1-47	CSI0_DAT6	IPU0_CSI0_D[6]		SPI1_MISO	KPD_COL6	AUD3_TXFS	GPIO5_24		
P1-48	CSI0_DAT4	IPU0_CSI0_D[4]		SPI1_CLK	KPD_COL5	AUD3_TXC	GPIO5_22		
P1-49	CSI0_DAT7	IPU0_CSI0_D[7]		SPI1_CS0	KPD_ROW6	AUD3_RXD	GPIO5_25		
P1-51	CSI0_MCLK	IPU0_CSI0_HSYNC					GPIO5_19		
P1-53	CSI0_VSYNC	IPU0_CSI0_VSYNC					GPIO5_21		
P1-56	GPIO_4	ESAI_HCKT		KPD_COL7			GPIO1_4	MMC2_CD	
P1-57	CSI0_PIXCLK	IPU0_CSI0_PIXCLK					GPIO5_18		
P1-58	GPIO_2	ESAI_FST		KPD_ROW6			GPIO1_2	MMC2_WP	MLBDAT
P1-59	CSI0_DATA_EN	IPU0_CSI0_DATA_EN					GPIO5_20		
P1-60	DI0_PIN4			AUD6_RXD	MMC1_WP		GPIO4_20		
P1-61	GPIO_8	ESAI_TX5_RX0		EPIT2_OUT	CAN1_RX	UART2_RX	GPIO1_8		
P1-63	EIM_OE			SPI2_MISO			GPIO2_25		
P1-64	KEY_COL1	SPI1_MISO		AUD5_TXFS	KPD_COL1	UART5_TX	GPIO4_8		
P1-65	EIM_D24		SPI4_CS2	UART3_TX	SPI1_CS2	SPI2_CS2	GPIO3_24	AUD5_RXFS	UART1_DTR
P1-66	KEY_ROW1	SPI1_CS0		AUD5_RXD	KPD_ROW1	UART5_RX	GPIO4_9		
P1-68	SD4_DAT5			UART2_RTS			GPIO2_13		
P1-69	EIM_CS1			SPI2_MOSI			GPIO2_24		
P1-70	SD4_DAT6			UART2_CTS			GPIO2_14		
P1-71	EIM_CS0			SPI2_CLK			GPIO2_23		
P1-72	GPIO_7	ESAI_TX4_RX1	SPI5_RDY	EPIT1_OUT	CAN1_TX	UART2_TX	GPIO1_7		
P1-73	EIM_D25		SPI4_CS3	UART3_RX	SPI1_CS3	SPI2_CS3	GPIO3_25	AUD5_RXC	UART1_DSR
P1-75	DISP0_DAT0	DISP0_DAT[0]	DISP0_DAT[0]	SPI3_CLK			GPIO4_21		
P1-76	DISP0_DAT1	DISP0_DAT[1]	DISP0_DAT[1]	SPI3_MOSI			GPIO4_22		
P1-77	DISP0_DAT2	DISP0_DAT[2]	DISP0_DAT[2]	SPI3_MISO			GPIO4_23		
P1-78	DISP0_DAT3	DISP0_DAT[3]	DISP0_DAT[3]	SPI3_CS0			GPIO4_24		
P1-81	DISP0_DAT4	DISP0_DAT[4]	DISP0_DAT[4]	SPI3_CS1			GPIO4_25		
P1-82	DISP0_DAT5	DISP0_DAT[5]	DISP0_DAT[5]	SPI3_CS2	AUD6_RXFS		GPIO4_26		
P1-83	DISP0_DAT6	DISP0_DAT[6]	DISP0_DAT[6]	SPI3_CS3	AUD6_RXC		GPIO4_27		
P1-84	DISP0_DAT7	DISP0_DAT[7]	DISP0_DAT[7]	SPI3_RDY			GPIO4_28		
P1-85	DISP0_DAT8	DISP0_DAT[8]	DISP0_DAT[8]	PWM1_OUT	WDOG1		GPIO4_29		
P1-87	DISP0_DAT9	DISP0_DAT[9]	DISP0_DAT[9]	PWM2_OUT	WDOG2		GPIO4_30		
P1-88	DISP0_DAT10	DISP0_DAT[10]	DISP0_DAT[10]				GPIO4_31		
P1-89	DISP0_DAT11	DISP0_DAT[11]	DISP0_DAT[11]				GPIO5_5		
P1-90	DISP0_DAT12	DISP0_DAT[12]	DISP0_DAT[12]				GPIO5_6		
P1-92	DISP0_DAT13	DISP0_DAT[13]	DISP0_DAT[13]		AUD5_RXFS		GPIO5_7		

Pin #	i.MX6 PAD	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
P1-93	DISP0_DAT14	DISP0_DAT[14]	DISP0_DAT[14]		AUD5_RXC		GPIO5_8		
P1-94	DISP0_DAT15	DISP0_DAT[15]	DISP0_DAT[15]	SPI1_CS1	SPI2_CS1		GPIO5_9		
P1-95	DISP0_DAT16	DISP0_DAT[16]	DISP0_DAT[16]	SPI2_MOSI	AUD5_TXC	SDMA_EXT_EVT0	GPIO5_10		
P1-96	DISP0_DAT17	DISP0_DAT[17]	DISP0_DAT[17]	SPI2_MISO	AUD5_TXD	SDMA_EXT_EVT1	GPIO5_11		
P1-97	DISP0_DAT18	DISP0_DAT[18]	DISP0_DAT[18]	SPI2_CS0	AUD5_TXFS	AUD4_RXFS	GPIO5_12		
P1-99	DISP0_DAT19	DISP0_DAT[19]	DISP0_DAT[19]	SPI2_CLK	AUD5_RXD	AUD4_RXC	GPIO5_13		
P1-100	DISP0_DAT20	DISP0_DAT[20]	DISP0_DAT[20]	SPI1_CLK	AUD4_TXC		GPIO5_14		
P1-101	DISP0_DAT21	DISP0_DAT[21]	DISP0_DAT[21]	SPI1_MOSI	AUD4_TXD		GPIO5_15		
P1-102	DISP0_DAT22	DISP0_DAT[22]	DISP0_DAT[22]	SPI1_MISO	AUD4_TXFS		GPIO5_16		
P1-104	DISP0_DAT23	DISP0_DAT[23]	DISP0_DAT[23]	SPI1_CS0	AUD4_RXD		GPIO5_17		
P1-105	DI0_PIN15	DI0_PIN15	DI0_PIN15	AUD6_TXC			GPIO4_17		
P1-107	DI0_PIN3	DI0_PIN3	DI0_PIN3	AUD6_TXFS			GPIO4_19		
P1-108	DI0_DISP_CLK	DI0_DISP_CLK	DI0_DISP_CLK				GPIO4_16		
P1-109	DI0_PIN2	DI0_PIN2	DI0_PIN2	AUD6_TXD			GPIO4_18		
P1-112	SD3_DAT6	MMC3_DAT6	UART1_RX				GPIO6_18		
P1-114	SD3_DAT7	MMC3_DAT7	UART1_TX				GPIO6_17		
P1-116	KEY_COL3	SPI1_CS3		DDC_SCL	KPD_COL3	I2C2_SCL	GPIO4_12	SPDIF_IN	
P1-124	GPIO_0			KPD_COL5		EPIT1_OUT	GPIO1_0	USB1_CPEN	
P1-125	KEY_ROW3			DDC_SDA	KPD_ROW3	I2C2_SDA	GPIO4_13		
P2-5	KEY_COL2	SPI1_CS1		CAN1_TX	KPD_COL2		GPIO4_10		
P2-6	KEY_ROW2	SPI1_CS2		CAN1_RX	KPD_ROW2		GPIO4_11	HDMI_CEC	
P2-13	SD3_DAT4	MMC3_DAT4	UART2_RX				GPIO7_1		
P2-20	ENET_RXD1	MLBSIG		ESAI_FST			GPIO1_26		
P2-25	EIM_D28		I2C1_SDA	SPI4_MOSI		UART2_CTS	GPIO3_28		
P2-27	EIM_D21		SPI4_CLK			USBOTG_OC	GPIO3_21	I2C1_SCL	SPDIF_IN
P2-29	SD4_DAT2			PWM4_OUT			GPIO2_10		
P2-39	ENET_TXD1	MLBCLK		ESAI_TX2_RX3			GPIO1_29		
P2-40	SD4_DAT1			PWM3_OUT			GPIO2_9		
P2-41	SD3_DAT5	MMC3_DAT5	UART2_TX				GPIO7_0		
P2-45	SD2_DAT3	MMC2_DAT3	SPI5_CS3	KPD_COL6	AUD4_TXC		GPIO1_12		
P2-47	SD2_DAT0	MMC2_DAT0	SPI5_MISO		AUD4_RXD	KPD_ROW7	GPIO1_15		
P2-49	SD2_DAT2	MMC2_DAT2	SPI5_CS1		AUD4_TXD	KPD_ROW6	GPIO1_13		
P2-51	SD2_DAT1	MMC2_DAT1	SPI5_CS0		AUD4_TXFS	KPD_COL7	GPIO1_14		
P2-53	GPIO_5	ESAI_TX2_RX3		KPD_ROW7			GPIO1_5	I2C3_SCL	
P2-54	SD3_DAT0	MMC3_DAT0	UART1_CTS	CAN2_TX			GPIO7_4		
P2-56	SD3_DAT1	MMC3_DAT1	UART1_RTS	CAN2_RX			GPIO7_5		
P2-57	SD2_CMD	MMC2_CMD	SPI5_MOSI	KPD_ROW5	AUD4_RXC		GPIO1_11		
P2-58	SD3_DAT2	MMC3_DAT2					GPIO7_6		
P2-59	SD2_CLK	MMC2_CLK	SPI5_CLK	KPD_COL5	AUD4_RXFS		GPIO1_10		
P2-60	SD3_DAT3	MMC3_DAT3	UART3_CTS				GPIO7_7		
P2-61	SD1_DAT0	MMC1_DAT0	SPI5_MISO		GPT_CAPIN1		GPIO1_16		
P2-63	SD1_DAT1	MMC1_DAT1	SPI5_CS0	PWM3_OUT	GPT_CAPIN2		GPIO1_17		
P2-64	CSI0_DAT12	IPU0_CSI0_D[12]			UART4_TX		GPIO5_30		
P2-65	SD1_DAT2	MMC1_DAT2	SPI5_CS1	GPT_CMPOUT2	PWM2_OUT	WDOG1	GPIO1_19	WDOG1_RST	
P2-66	CSI0_DAT13	IPU0_CSI0_D[13]			UART4_RX		GPIO5_31		
P2-68	CSI0_DAT14	IPU0_CSI0_D[14]			UART5_TX		GPIO6_0		
P2-69	SD1_DAT3	MMC1_DAT3	SPI5_CS2	GPT_CMPOUT3	PWM1_OUT	WDOG2	GPIO1_21	WDOG2_RST	
P2-70	CSI0_DAT15	IPU0_CSI0_D[15]			UART5_RX		GPIO6_1		
P2-71	GPIO_1	ESAI_SCKR	WDOG2	KPD_ROW5	USBOTG_ID	PWM2_OUT	GPIO1_1	MMC1_CD	
P2-72	CSI0_DAT16	IPU0_CSI0_D[16]			UART4_RTS		GPIO6_2		
P2-73	SD1_CLK	MMC1_CLK	SPI5_CLK		GPT_CLKIN		GPIO1_20		
P2-75	SD1_CMD	MMC1_CMD	SPI5_MOSI	PWM4_OUT	GPT_CMPOUT1		GPIO1_18		
P2-76	SD3_CLK	MMC3_CLK	UART2_RTS	CAN1_RX			GPIO7_3		
P2-77	GPIO_9	ESAI_FSR	WDOG1	KPD_COL6		PWM1_OUT	GPIO1_9	MMC1_WP	
P2-78	SD3_CMD	MMC3_CMD	UART2_CTS	CAN1_TX			GPIO7_2		
P2-80	CSI0_DAT17	IPU0_CSI0_D[17]			UART4_CTS		GPIO6_3		
P2-82	CSI0_DAT18	IPU0_CSI0_D[18]			UART5_RTS		GPIO6_4		
P2-84	CSI0_DAT19	IPU0_CSI0_D[19]			UART5_CTS		GPIO6_5		
P2-85	KEY_COL4	CAN2_TX		USBOTG_OC	KPD_COL4	UART5_RTS	GPIO4_14		
P2-87	KEY_ROW4	CAN2_RX		USBOTG_CPEN	KPD_ROW4	UART5_CTS	GPIO4_15		
P2-89	ENET_CRS_DV			ESAI_SCKT			GPIO1_25		
P2-97	NANDF_CS2			ESAI_TX0			GPIO6_15		
P2-104	EIM_D22		SPI4_MISO			USBOTG_CPEN	GPIO3_22	SPDIF_OUT	
P2-119	GPIO_18	ESAI_TX1			SDMA_EXT_EVT1		GPIO7_13		
P2-121	ENET_RXD0			ESAI_HCKT	SPDIF_OUT		GPIO1_27		
P2-128	ENET_RX_ER	USBOTG_ID		ESAI_HCKR	SPDIF_IN		GPIO1_24		

5.6 RTC

The CM-FX6 RTC is implemented with the internal RTC of the i.MX6 SoC. The RTC provides time and calendar information.

Additionally, a backup battery can keep the RTC running to maintain clock and time information even if the main supply is not present. If the backup battery is rechargeable, the device also provides a backup battery charger so it can be recharged when the main battery supply is present. The backup battery should be connected to the VCC_RTC power input.

NOTE: VCC_RTC must remain valid at all times for proper operation of the on-board RTC.

5.7 LED

The CM-FX6 features a single general purpose green LED controlled by GPIO2_31 signal of the i.MX6 SoC. The LED is ON when GPIO2_31 is set high.

6 CARRIER BOARD INTERFACE

The CM-FX6 connects to the carrier board through P1 and P2 - 0.6 mm pitch 140-pin connectors.

6.1 Connector Pinout

Table 50 Connector P1

Pin #	CM-FX6 Signal Name	Reference Section		Pin #	CM-FX6 Signal Name	Reference Section
P1-1	ETH_MDI1P	4.8		P1-2	ETH_MDI0P	4.8
P1-3	ETH_MDI1N	4.8		P1-4	ETH_MDI0N	4.8
P1-5	ETH_LED2	4.8		P1-6	ETH_LED1	4.8
P1-7	V_ROOT	5.1.1		P1-8	GND	5.1.1
P1-9	ETH_MDI3P	4.8		P1-10	ETH_MDI2P	4.8
P1-11	ETH_MDI3N	4.8		P1-12	ETH_MDI2N	4.8
P1-13	ETH_LED3	4.8		P1-14	GND	5.1.1
P1-15	LVDS0_CLK_N	4.3.1.2		P1-16	LVDS0_TX0_N	4.3.1.2
P1-17	LVDS0_CLK_P	4.3.1.2		P1-18	LVDS0_TX0_P	4.3.1.2
P1-19	V_ROOT	5.1.1		P1-20	ESAI_TX3_RX2 MMC1_LCTL SPDIF_IN GPIO7_11 I2C3_SDA	4.4.2.2 4.12 4.4.2.1 4.15 4.16
P1-21	TS_X-	4.13		P1-22	LVDS0_TX1_N	4.3.1.2
P1-23	TS_X+	4.13		P1-24	LVDS0_TX1_P	4.3.1.2
P1-25	JTAG_MOD	4.23		P1-26	GND	5.1.1
P1-27	TS_Y-	4.13		P1-28	LVDS0_TX2_N	4.3.1.2
P1-29	TS_Y+	4.13		P1-30	LVDS0_TX2_P	4.3.1.2
P1-31	V_ROOT	5.1.1		P1-32	KPD_COL5 SPDIF_OUT SPI1_RDY GPIO4_5	4.14 4.4.2.1 4.17 4.15
P1-33	IPU0_CSI0_D[8] SPI2_CLK KPD_COL7 I2C1_SDA GPIO5_26	4.3.3.1 4.17 4.14 4.16 4.15		P1-34	LVDS0_TX3_N	4.3.1.2
P1-35	IPU0_CSI0_D[9] SPI2_MOSI KPD_ROW7 I2C1_SCL GPIO5_27	4.3.3.1 4.17 4.14 4.16 4.15		P1-36	LVDS0_TX3_P	4.3.1.2
P1-37	VCC_RTC	5.1.1		P1-38	GND	5.1.1
P1-39	IPU0_CSI0_D[10] AUD3_RXC SPI2_MISO UART1_TX GPIO5_28	4.3.3.1 4.4.2.3 4.17 4.10 4.15		P1-40	IPU0_CSI0_D[0] UART2_RX GPIO3_27	4.3.3.1 4.10 4.15
P1-41	IPU0_CSI0_D[11] AUD3_RXFS SPI2_CS0 UART1_RX GPIO5_29	4.3.3.1 4.4.2.3 4.17 4.10 4.15		P1-42	IPU0_CSI0_D[1] UART2_TX GPIO3_26	4.3.3.1 4.10 4.15
P1-43	V_ROOT	5.1.1		P1-44	IPU0_CSI0_D[2] UART3_RTS GPIO3_31 USB1_CPEN	4.3.3.1 4.10 4.15 4.9.2
P1-45	IPU0_CSI0_D[5] SPI1_MOSI KPD_ROW5 AUD3_TXD GPIO5_23	4.3.3.1 4.17 4.14 4.4.2.3 4.15		P1-46	IPU0_CSI0_D[3] UART3_CTS GPIO3_30 USB1_nOVC	4.3.3.1 4.10 4.15 4.9.2

Pin #	CM-FX6 Signal Name	Reference Section	Pin #	CM-FX6 Signal Name	Reference Section
P1-47	IPU0_CSI0_D[6] SPI1_MISO KPD_COL6 AUD3_TXFS GPIO5_24	4.3.3.1 4.17 4.14 4.4.2.3 4.15	P1-48	IPU0_CSI0_D[4] SPI1_CLK KPD_COL5 AUD3_TXC GPIO5_22	4.3.3.1 4.17 4.14 4.4.2.3 4.15
P1-49	IPU0_CSI0_D[7] SPI1_CS0 KPD_ROW6 AUD3_RXD GPIO5_25	4.3.3.1 4.17 4.14 4.4.2.3 4.15	P1-50	GND	5.1.1
P1-51	IPU0_CSI0_HSYNC GPIO5_19	4.3.3.1 4.15	P1-52	GENP_LVDSCLK2_DN	5.4.3
P1-53	IPU0_CSI0_VSYNC GPIO5_21	4.3.3.1 4.15	P1-54	GENP_LVDSCLK2_DP	5.4.3
P1-55	V_ROOT	5.1.1	P1-56	ESAI_HCKT KPD_COL7 GPIO1_4 MMC2_CD	4.4.2.2 4.14 4.15 4.12
P1-57	IPU0_CSI0_PIXCLK GPIO5_18	4.3.3.1 4.15	P1-58	ESAI_FST KPD_ROW6 GPIO1_2 MMC2_WP MLBDAT	4.4.2.2 4.14 4.15 4.12 4.7
P1-59	IPU0_CSI0_DATA_EN GPIO5_20	4.3.3.1 4.15	P1-60	AUD6_RXD MMC1_WP GPIO4_20	4.4.2.3 4.12 4.15
P1-61	ESAI_TX5_RX0 EPIT2_OUT CAN1_RX UART2_RX GPIO1_8	4.4.2.2 4.20 4.18 4.10 4.15	P1-62	GND	5.1.1
P1-63	SPI2_MISO GPIO2_25	4.17 4.15	P1-64	SPI1_MISO AUD5_TXFS KPD_COL1 UART5_TX GPIO4_8	4.17 4.4.2.3 4.14 4.10 4.15
P1-65	SPI4_CS2 UART3_TX SPI1_CS2 SPI2_CS2 GPIO3_24 AUD5_RXFS UART1_DTR	4.17 4.10 4.17 4.17 4.15 4.4.2.3	P1-66	SPI1_CS0 AUD5_RXD KPD_ROW1 UART5_RX GPIO4_9	4.17 4.4.2.3 4.14 4.10 4.15
P1-67	V_ROOT	5.1.1	P1-68	UART2_RTS GPIO2_13	4.10 4.15
P1-69	SPI2_MOSI GPIO2_24	4.17 4.15	P1-70	UART2_CTS GPIO2_14	4.10 4.15
P1-71	SPI2_CLK GPIO2_23	4.17 4.15	P1-72	ESAI_TX4_RX1 SPI5_RDY EPIT1_OUT CAN1_TX UART2_TX GPIO1_7	4.4.2.2 4.17 4.20 4.18 4.10 4.15
P1-73	SPI4_CS3 UART3_RX SPI1_CS3 SPI2_CS3 GPIO3_25 AUD5_RXC UART1_DSR	4.17 4.10 4.17 4.17 4.15 4.4.2.3 4.10	P1-74	GND	5.1.1
P1-75	DISP0_DAT[0] DISP0_DAT[0] SPI3_CLK GPIO4_21	4.3.1.1 4.3.1.1 4.17 4.15	P1-76	DISP0_DAT[1] DISP0_DAT[1] SPI3_MOSI GPIO4_22	4.3.1.1 4.3.1.1 4.17 4.15
P1-77	DISP0_DAT[2] DISP0_DAT[2] SPI3_MISO GPIO4_23	4.3.1.1 4.3.1.1 4.17 4.15	P1-78	DISP0_DAT[3] DISP0_DAT[3] SPI3_CS0 GPIO4_24	4.3.1.1 4.3.1.1 4.17 4.15
P1-79	V_ROOT	5.1.1	P1-80	USBOTG_nCHD	4.9.1

Pin #	CM-FX6 Signal Name	Reference Section		Pin #	CM-FX6 Signal Name	Reference Section
P1-81	DISP0_DAT[4] DISP0_DAT[4] SPI3_CS1 GPIO4_25	4.3.1.1 4.3.1.1 4.17 4.15		P1-82	DISP0_DAT[5] DISP0_DAT[5] SPI3_CS2 AUD6_RXFS GPIO4_26	4.3.1.1 4.3.1.1 4.17 4.4.2.3 4.15
P1-83	DISP0_DAT[6] DISP0_DAT[6] SPI3_CS3 AUD6_RXC GPIO4_27	4.3.1.1 4.3.1.1 4.17 4.4.2.3 4.15		P1-84	DISP0_DAT[7] DISP0_DAT[7] SPI3_RDY GPIO4_28	4.3.1.1 4.3.1.1 4.17 4.15
P1-85	DISP0_DAT[8] DISP0_DAT[8] PWM1_OUT WDOG1 GPIO4_29	4.3.1.1 4.3.1.1 4.21 4.22 4.15		P1-86	GND	5.1.1
P1-87	DISP0_DAT[9] DISP0_DAT[9] PWM2_OUT WDOG2 GPIO4_30	4.3.1.1 4.3.1.1 4.21 4.22 4.15		P1-88	DISP0_DAT[10] DISP0_DAT[10] GPIO4_31	4.3.1.1 4.3.1.1 4.15
P1-89	DISP0_DAT[11] DISP0_DAT[11] GPIO5_5	4.3.1.1 4.3.1.1 4.15		P1-90	DISP0_DAT[12] DISP0_DAT[12] GPIO5_6	4.3.1.1 4.3.1.1 4.15
P1-91	V_ROOT	5.1.1		P1-92	DISP0_DAT[13] DISP0_DAT[13] AUD5_RXFS GPIO5_7	4.3.1.1 4.3.1.1 4.4.2.3 4.15
P1-93	DISP0_DAT[14] DISP0_DAT[14] AUD5_RXC GPIO5_8	4.3.1.1 4.3.1.1 4.4.2.3 4.15		P1-94	DISP0_DAT[15] DISP0_DAT[15] SPI1_CS1 SPI2_CS1 GPIO5_9	4.3.1.1 4.3.1.1 4.17 4.17 4.15
P1-95	DISP0_DAT[16] DISP0_DAT[16] SPI2_MOSI AUD5_TXC SDMA_EXT_EVT0 GPIO5_10	4.3.1.1 4.3.1.1 4.17 4.4.2.3 5.4.1 4.15		P1-96	DISP0_DAT[17] DISP0_DAT[17] SPI2_MISO AUD5_TXD SDMA_EXT_EVT1 GPIO5_11	4.3.1.1 4.3.1.1 4.17 4.4.2.3 5.4.1 4.15
P1-97	DISP0_DAT[18] DISP0_DAT[18] SPI2_CS0 AUD5_TXFS AUD4_RXFS GPIO5_12	4.3.1.1 4.3.1.1 4.17 4.4.2.3 4.4.2.3 4.15		P1-98	GND	5.1.1
P1-99	DISP0_DAT[19] DISP0_DAT[19] SPI2_CLK AUD5_RXD AUD4_RXC GPIO5_13	4.3.1.1 4.3.1.1 4.17 4.4.2.3 4.4.2.3 4.15		P1-100	DISP0_DAT[20] DISP0_DAT[20] SPI1_CLK AUD4_TXC GPIO5_14	4.3.1.1 4.3.1.1 4.17 4.4.2.3 4.15
P1-101	DISP0_DAT[21] DISP0_DAT[21] SPI1_MOSI AUD4_TXD GPIO5_15	4.3.1.1 4.3.1.1 4.17 4.4.2.3 4.15		P1-102	DISP0_DAT[22] DISP0_DAT[22] SPI1_MISO AUD4_TXFS GPIO5_16	4.3.1.1 4.3.1.1 4.17 4.4.2.3 4.15
P1-103	V_ROOT	5.1.1		P1-104	DISP0_DAT[23] DISP0_DAT[23] SPI1_CS0 AUD4_RXD GPIO5_17	4.3.1.1 4.3.1.1 4.17 4.4.2.3 4.15
P1-105	DI0_PIN15 DI0_PIN15 AUD6_TXC GPIO4_17	4.3.1.1 4.3.1.1 4.4.2.3 4.15		P1-106	USB1_nOVC	4.9.2
P1-107	DI0_PIN3 DI0_PIN3 AUD6_TXFS GPIO4_19	4.3.1.1 4.3.1.1 4.4.2.3 4.15		P1-108	DI0_DISP_CLK DI0_DISP_CLK GPIO4_16	4.3.1.1 4.3.1.1 4.15

Pin #	CM-FX6 Signal Name	Reference Section		Pin #	CM-FX6 Signal Name	Reference Section
P1-109	DI0_PIN2 DI0_PIN2 AUD6_TXD GPIO4_18	4.3.1.1 4.3.1.1 4.4.2.3 4.15		P1-110	GND	5.1.1
P1-111	CSI_D3M	4.3.3.2		P1-112	MMC3_DAT6 UART1_RX GPIO6_18	4.12 4.10 4.15
P1-113	CSI_D3P	4.3.3.2		P1-114	MMC3_DAT7 UART1_TX GPIO6_17	4.12 4.10 4.15
P1-115	V_ROOT	5.1.1		P1-116	SPI1_CS3 DDC_SCL KPD_COL3 I2C2_SCL GPIO4_12 SPDIF_IN	4.17 4.5 4.14 4.16 4.15 4.4.2.1
P1-117	RS232_RXD	4.11		P1-118	CSI_D1M	4.3.3.2
P1-119	RS232_TXD	4.11		P1-120	CSI_D1P	4.3.3.2
P1-121	CSI_D2M	4.3.3.2		P1-122	GND	5.1.1
P1-123	CSI_D2P	4.3.3.2		P1-124	KPD_COL5 EPIT1_OUT GPIO1_0 USB1_CPEN	4.14 4.20 4.15 4.9.2
P1-125	DDC_SDA KPD_ROW3 I2C2_SDA GPIO4_13	4.5 4.14 4.16 4.15		P1-126	USB3_CPEN	4.9.2
P1-127	V_ROOT	5.1.1		P1-128	USB2_CPEN	4.9.2
P1-129	USB3_DN	4.9.2		P1-130	USB1_DN	4.9.2
P1-131	USB3_DP	4.9.2		P1-132	USB1_DP	4.9.2
P1-133	USB4_CPEN	4.9.2		P1-134	GND	5.1.1
P1-135	USB4_DN	4.9.2		P1-136	USB2_DN	4.9.2
P1-137	USB4_DP	4.9.2		P1-138	USB2_DP	4.9.2
P1-139	V_ROOT	5.1.1		P1-140	USB1_VBUS	4.9.2

Table 51 Connector P2

Pin #	CM-FX6 Signal Name	Reference Section		Pin #	CM-FX6 Signal Name	Reference Section
P2-1	MLB_CP	4.7		P2-2	MLB_DP	4.7
P2-3	MLB_CN	4.7		P2-4	MLB_DN	4.7
P2-5	SPI1_CS1 CAN1_TX KPD_COL2 GPIO4_10	4.17 4.18 4.14 4.15		P2-6	SPI1_CS2 CAN1_RX KPD_ROW2 GPIO4_11 HDMI_CEC	4.17 4.18 4.14 4.15 4.5
P2-7	GND	5.1.1		P2-8	GND	5.1.1
P2-9	LVDS1_CLK_N	4.3.1.2		P2-10	MLB_SP	4.7
P2-11	LVDS1_CLK_P	4.3.1.2		P2-12	MLB_SN	4.7
P2-13	MMC3_DAT4 UART2_RX GPIO7_1	4.12 4.10 4.15		P2-14	GND	5.1.1
P2-15	LVDS1_TX2_N	4.3.1.2		P2-16	HDMI_TMDS_CLK_DN	4.5
P2-17	LVDS1_TX2_P	4.3.1.2		P2-18	HDMI_TMDS_CLK_DP	4.5
P2-19	V_ROOT	5.1.1		P2-20	MLBSIG ESAI_FST GPIO1_26	4.7 4.4.2.2 4.15
P2-21	LVDS1_TX3_N	4.3.1.2		P2-22	HDMI_TMDS_DATA0_DN	4.5
P2-23	LVDS1_TX3_P	4.3.1.2		P2-24	HDMI_TMDS_DATA0_DP	4.5
P2-25	I2C1_SDA SPI4_MOSI UART2_CTS GPIO3_28	4.16 4.17 4.10 4.15		P2-26	GND	5.1.1
P2-27	SPI4_CLK USBOTG_OC GPIO3_21 I2C1_SCL SPDIF_IN	4.17 4.9.1 4.15 4.16 4.4.2.1		P2-28	LVDS1_TX0_N	4.3.1.2

Pin #	CM-FX6 Signal Name	Reference Section	Pin #	CM-FX6 Signal Name	Reference Section
P2-29	PWM4_OUT GPIO2_10	4.21 4.15	P2-30	LVDS1_TX0_P	4.3.1.2
P2-31	V_ROOT	5.1.1	P2-32	HDMI_HPD	
P2-33	nCOLD_RST	5.2	P2-34	LVDS1_TX1_N	4.3.1.2
P2-35	RESERVED		P2-36	LVDS1_TX1_P	4.3.1.2
P2-37	PMIC_ON_REQ	5.4.1	P2-38	GND	5.1.1
P2-39	MLBCLK ESAI_TX2_RX3 GPIO1_29	4.7 4.4.2.2 4.15	P2-40	PWM3_OUT GPIO2_9	4.21 4.15
P2-41	MMC3_DAT5 UART2_TX GPIO7_0	4.12 4.10 4.15	P2-42	HDMI_TMDS_DATA1_DN	4.5
P2-43	V_ROOT	5.1.1	P2-44	HDMI_TMDS_DATA1_DP	4.5
P2-45	MMC2_DAT3 SPI5_CS3 KPD_COL6 AUD4_TXC GPIO1_12	4.12 4.17 4.14 4.4.2.3 4.15	P2-46	FLASH_nWP	5.4.4
P2-47	MMC2_DAT0 SPI5_MISO AUD4_RXD KPD_ROW7 GPIO1_15	4.12 4.17 4.4.2.3 4.14 4.15	P2-48	HDMI_TMDS_DATA2_DN	4.5
P2-49	MMC2_DAT2 SPI5_CS1 AUD4_TXD KPD_ROW6 GPIO1_13	4.12 4.17 4.4.2.3 4.14 4.15	P2-50	HDMI_TMDS_DATA2_DP	4.5
P2-51	MMC2_DAT1 SPI5_CS0 AUD4_TXFS KPD_COL7 GPIO1_14	4.12 4.17 4.4.2.3 4.14 4.15	P2-52	GND	5.1.1
P2-53	ESAI_TX2_RX3 KPD_ROW7 GPIO1_5 I2C3_SCL	4.4.2.2 4.14 4.15 4.16	P2-54	MMC3_DAT0 UART1_CTS CAN2_TX GPIO7_4	4.12 4.10 4.18 4.15
P2-55	V_ROOT	5.1.1	P2-56	MMC3_DAT1 UART1_RTS CAN2_RX GPIO7_5	4.12 4.10 4.18 4.15
P2-57	MMC2_CMD SPI5_MOSI KPD_ROW5 AUD4_RXC GPIO1_11	4.12 4.17 4.14 4.4.2.3 4.15	P2-58	MMC3_DAT2 GPIO7_6	4.12 4.15
P2-59	MMC2_CLK SPI5_CLK KPD_COL5 AUD4_RXFS GPIO1_10	4.12 4.17 4.14 4.4.2.3 4.15	P2-60	MMC3_DAT3 UART3_CTS GPIO7_7	4.12 4.10 4.15
P2-61	MMC1_DAT0 SPI5_MISO GPT_CAPIN1 GPIO1_16	4.12 4.17 4.19 4.15	P2-62	GND	5.1.1
P2-63	MMC1_DAT1 SPI5_CS0 PWM3_OUT GPT_CAPIN2 GPIO1_17	4.12 4.17 4.21 4.19 4.15	P2-64	IPU0_CSI0_D[12] UART4_TX GPIO5_30	4.3.3.1 4.10 4.15
P2-65	MMC1_DAT2 SPI5_CS1 GPT_CMPOUT2 PWM2_OUT WDOG1 GPIO1_19 WDOG1_RST	4.12 4.17 4.19 4.21 4.22 4.15 4.22	P2-66	IPU0_CSI0_D[13] UART4_RX GPIO5_31	4.3.3.1 4.10 4.15

Pin #	CM-FX6 Signal Name	Reference Section	Pin #	CM-FX6 Signal Name	Reference Section
P2-67	V_ROOT	5.1.1	P2-68	IPU0_CSI0_D[14] UART5_TX GPIO6_0	4.3.3.1 4.10 4.15
P2-69	MMC1_DAT3 SPI5_CS2 GPT_CMPOUT3 PWM1_OUT WDOG2 GPIO1_21 WDOG2_RST	4.12 4.17 4.19 4.21 4.22 4.15 4.22	P2-70	IPU0_CSI0_D[15] UART5_RX GPIO6_1	4.3.3.1 4.10 4.15
P2-71	ESAI_SCKR WDOG2 KPD_ROW5 USBOTG_ID PWM2_OUT GPIO1_1 MMC1_CD	4.4.2.2 4.22 4.14 4.9.1 4.21 4.15 4.12	P2-72	IPU0_CSI0_D[16] UART4_RTS GPIO6_2	4.3.3.1 4.10 4.15
P2-73	MMC1_CLK SPI5_CLK GPT_CLKIN GPIO1_20	4.12 4.17 4.19 4.15	P2-74	GND	5.1.1
P2-75	MMC1_CMD SPI5_MOSI PWM4_OUT GPT_CMPOUT1 GPIO1_18	4.12 4.17 4.21 4.19 4.15	P2-76	MMC3_CLK UART2_RTS CAN1_RX GPIO7_3	4.12 4.10 4.18 4.15
P2-77	ESAI_FSR WDOG1 KPD_COL6 PWM1_OUT GPIO1_9 MMC1_WP	4.4.2.2 4.22 4.14 4.21 4.15 4.12	P2-78	MMC3_CMD UART2_CTS CAN1_TX GPIO7_2	4.12 4.10 4.18 4.15
P2-79	V_ROOT	5.1.1	P2-80	IPU0_CSI0_D[17] UART4_CTS GPIO6_3	4.3.3.1 4.10 4.15
P2-81	DSI_CLK_N	4.3.1.3	P2-82	IPU0_CSI0_D[18] UART5_RTS GPIO6_4	4.3.3.1 4.10 4.15
P2-83	DSI_CLK_P	4.3.1.3	P2-84	IPU0_CSI0_D[19] UART5_CTS GPIO6_5	4.3.3.1 4.10 4.15
P2-85	CAN2_TX USBOTG_OC KPD_COL4 UART5_RTS GPIO4_14	4.18 4.9.1 4.14 4.10 4.15	P2-86	GND	5.1.1
P2-87	CAN2_RX USBOTG_CPEN KPD_ROW4 UART5_CTS GPIO4_15	4.18 4.9.1 4.14 4.10 4.15	P2-88	JTAG_nTRST	4.23
P2-89	ESAI_SCKT GPIO1_25	4.4.2.2 4.15	P2-90	JTAG_TCK	4.23
P2-91	V_ROOT	5.1.1	P2-92	JTAG_TDI	4.23
P2-93	CSI_D0M	4.3.3.2	P2-94	JTAG_TDO	4.23
P2-95	CSI_D0P	4.3.3.2	P2-96	JTAG_TMS	4.23
P2-97	ESAI_TX0 GPIO6_15	4.4.2.2 4.15	P2-98	GND	5.1.1
P2-99	GENP_LVDSCLK1_DN	5.4.3	P2-100	CSI_CLK0M	4.3.3.2
P2-101	GENP_LVDSCLK1_DP	5.4.3	P2-102	CSI_CLK0P	4.3.3.2
P2-103	V_ROOT	5.1.1	P2-104	SPI4_MISO USBOTG_CPEN GPIO3_22 SPDIF_OUT	4.17 4.9.1 4.15 4.4.2.1
P2-105	DSI_D0_N	4.3.1.3	P2-106	PCIE_RXM	4.1
P2-107	DSI_D0_P	4.3.1.3	P2-108	PCIE_RXP	4.1
P2-109	PMIC_STBY_REQ	5.4.1	P2-110	GND	5.1.1
P2-111	DSI_D1_N	4.3.1.3	P2-112	PCIE_TXM	4.1
P2-113	DSI_D1_P	4.3.1.3	P2-114	PCIE_TXP	4.1

Pin #	CM-FX6 Signal Name	Reference Section		Pin #	CM-FX6 Signal Name	Reference Section
P2-115	V_ROOT	5.1.1		P2-116	USBOTG_VBUS	4.9.1
P2-117	ALT_BOOT	5.3		P2-118	SATA_RXM	4.2
P2-119	ESAI_TX1 SDMA_EXT_EVT1 GPIO7_13	4.4.2.2 5.4.1 4.15		P2-120	SATA_RXP	4.2
P2-121	ESAI_HCKT SPDIF_OUT GPIO1_27	4.4.2.2 4.4.2.1 4.15		P2-122	GND	5.1.1
P2-123	ONB_SSD_nACT	5.4.5		P2-124	SATA_TXM	4.2
P2-125	MIC_BIAS	4.4.1		P2-126	SATA_TXP	4.2
P2-127	V_ROOT	5.1.1		P2-128	USBOTG_ID ESAI_HCKR SPDIF_IN GPIO1_24	4.9.1 4.4.2.2 4.4.2.1 4.15
P2-129	MIC_IN	4.4.1		P2-130	USBOTG_DN	4.9.1
P2-131	LINEIN_R	4.4.1		P2-132	USBOTG_DP	4.9.1
P2-133	LINEIN_L	4.4.1		P2-134	GND	5.1.1
P2-135	V_ROOT	5.1.1		P2-136	USB4_nOVC	4.9.2
P2-137	HP_OUT_R	4.4.1		P2-138	USB3_nOVC	4.9.2
P2-139	HP_OUT_L	4.4.1		P2-140	USB2_nOVC	4.9.2

6.2 Connector Type

Table 52 Connector type

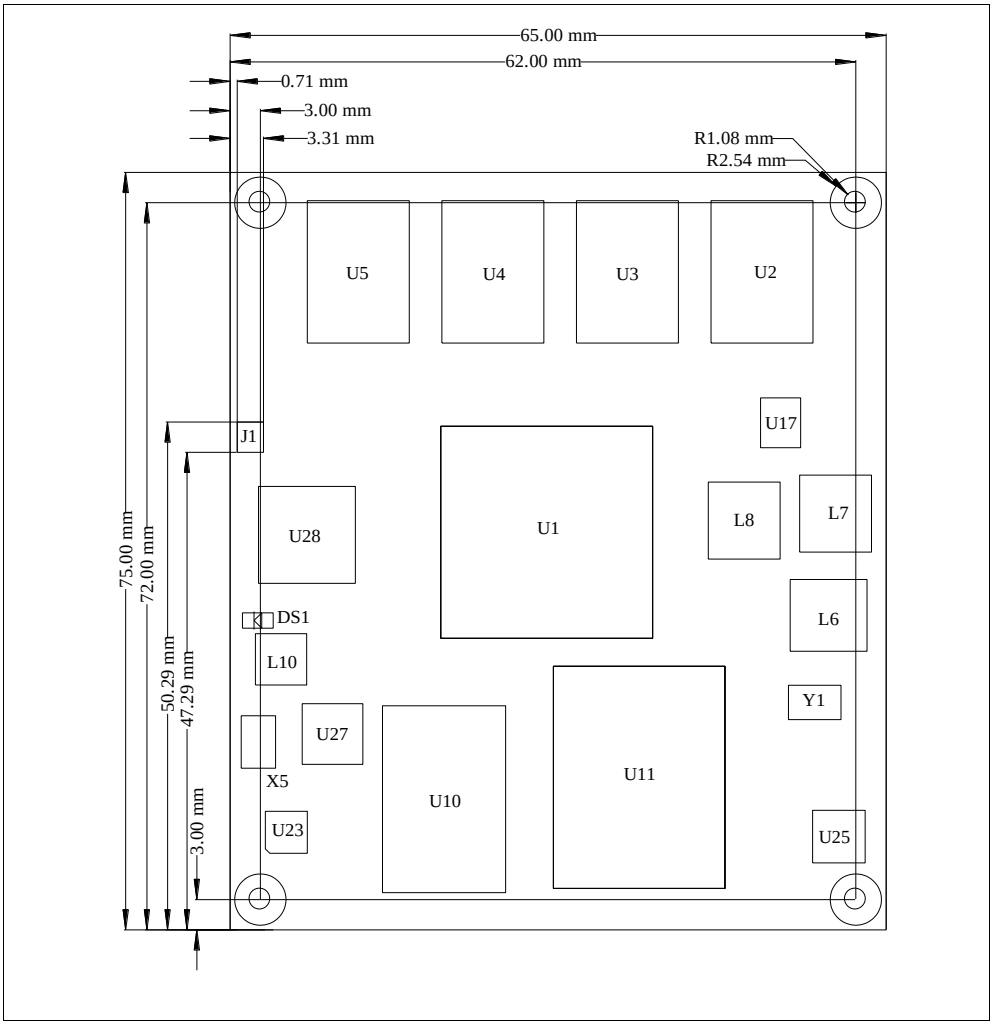
Part Reference	Mfg.	CM-FX6 connector P/N	Carrier board (mating) connector P/N
P1, P2	AMP	1-5353183-0	1-5353190-0 or CON140

Mating connectors and standoffs are available from CompuLab at:
http://compulab.co.il/support/cables-connectors-accessories/

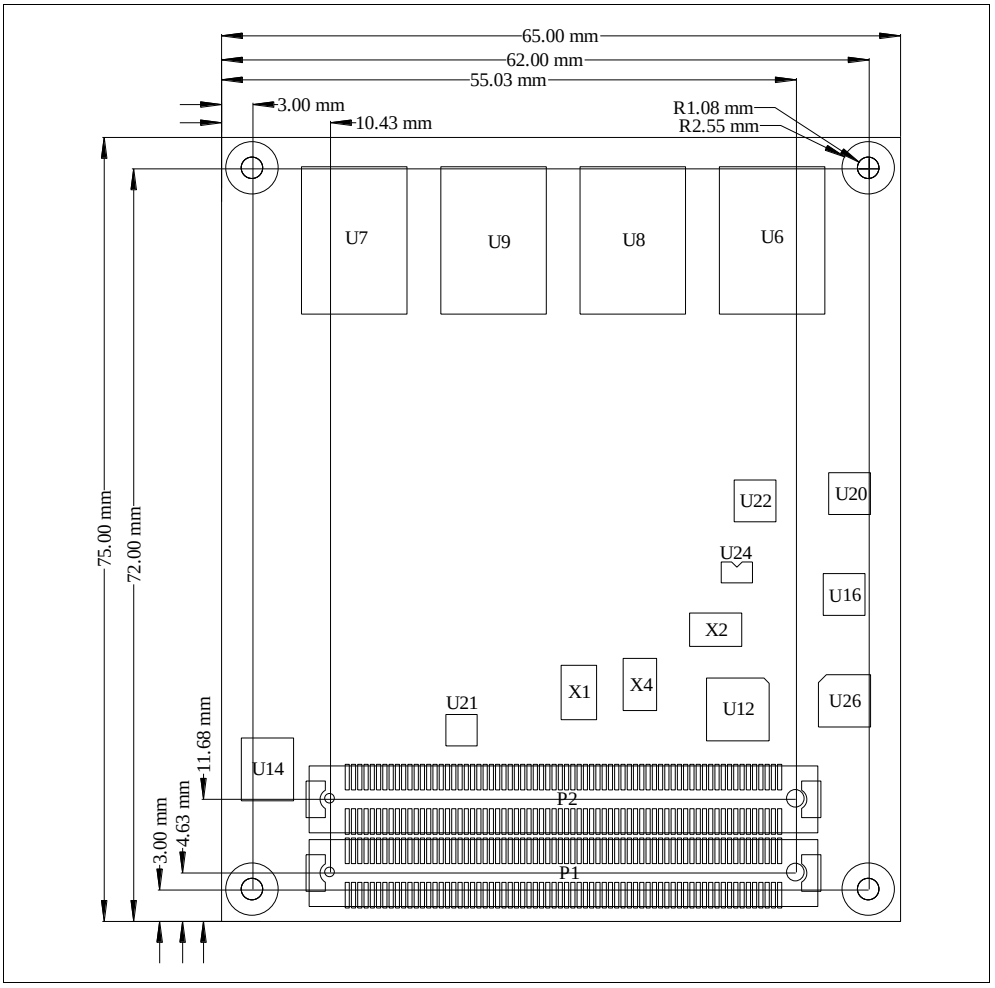
The CompuLab P/N for the AMP 1-5353190-0 connector is "CON140".

6.3 Mechanical Drawings

Figure 6 CM-FX6 Top



CM-FX6 bottom (X-Ray view - as seen from top side)



1. All dimensions are in millimeters.

2. Height of all components is < 3.5mm.

3. Baseboard connectors provide 4mm board-to-board clearance.

4. Board thickness is 1.6mm.

Mechanical drawings are available in DXF format at http://compulab.co.il/products/computer-on-modules/cm-fx6/#devres

6.4 Standoffs

The CM-FX6 has four mounting holes for standoffs. Standoffs are implemented with three parts: screw, spacer and nut.

Table 53 Standoffs

Part	Description	Manufacturer and P/N
Screw	M2, 10 mm length	• FCI 95121-005 • Acton InoxPro BF22102010 • World Bridge Machinery 380J52080
Spacer	M2 x 4 thread, 4.2 mm length	• Hirosugi ASU-2004 • MAC8 2SP-4 • World Bridge Machinery M2, L=4.2 mm
Nut	M2, 1.6-2.0mm width	• FCI 92869-001 (or 002) • Acton InoxPro BG12102000 • Bossard 1241397 (DIN934-A2 M2) • World Bridge Machinery 381A52000

7 OPERATIONAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

Table 54 Absolute Maximum ratings

Parameter	Limitations	Min	Typ	Max	Unit
Main power supply voltage (V_ROOT)		-0.3		6	V
Backup battery supply voltage (VCC_RTC)		2.8		3.3	V
USB VBUS		4.4		5.25	V

NOTE: Exceeding the absolute maximum ratings may damage the device.

7.2 Recommended Operating Conditions

Table 55 Recommended Operating Conditions

Parameter	Limitations	Min	Typ	Max	Unit
Main power supply voltage (V_ROOT)		3.3	5.0	5.5	V
Backup battery supply voltage (VCC_RTC)		2.8	3.0	3.3	V
USB VBUS		4.4		5.25	V

7.3 DC Electrical Characteristics

Table 56 DC Electrical Characteristics

Parameter	Operating Conditions	Min	Typ	Max	Unit
Multifunctional Digital I/O					
V_{IH}		2.31		3.3	V
V_{IL}		0		0.99	V
V_{OH}		3.15			V
V_{OL}				0.15	V
RS232					
TX Voltage Swing		-5.5		5.5	V
RX Voltage Swing		-25		25	V

NOTE: For LVDS, PCIe, HDMI and MIPI electrical characteristics, please refer to the i.MX6 datasheet.

7.4 ESD Performance

Table 57 ESD Performance

Interface	ESD Performance
RS232	15kV using Human Body Model (HBM)
Multifunctional pins	2kV using Human Body Model (HBM) / 0.5kV using Charge Device Model (CDM)
USB Host ports (with U5 option)	4kV using Human Body Model (HBM)

7.5 Operating Temperature Ranges

The CM-FX6 is available with three options of operating temperature range.

Table 58 CM-FX6 Temperature Range Options

Range	Temp.	Description
Commercial	0^{o} to 70^{o} C	Sample boards from each batch are tested for the lower and upper temperature limits. Individual boards are not tested.
Extended	-20^{o} to 70^{o} C	Every board undergoes a short test for the lower limit (-20^{o} C) qualification.
Industrial	-40^{o} to 85^{o} C	Every board is extensively tested for both lower and upper limits and at several midpoints.

8 APPLICATION NOTES

8.1 Carrier Board Design Guidelines

- Ensure that all V_ROOT and GND power pins are connected.
- Major power rails - V_ROOT and GND must be implemented by planes, rather than traces. Using at least two planes is essential to ensure the system signal quality, because the planes provide a current return path for all interface signals.
- It is recommended to put several 100nF and 10/100uF capacitors between V_ROOT and GND near the mating connectors.
- It is recommended to connect the standoff holes of the carrier board to GND, in order to improve EMC.
- Except for a power connection, no other connection is mandatory for CM-FX6 operation. All power-up circuitry and all required pullups/pulldowns are found on the module.
- If for some reason you decide to place an external pullup or pulldown resistor on a certain signal (for example - on the GPIOs), first check the documentation of that signal provided in this manual. Certain signals have on-board pullup/pulldown resistors required for proper initialization. Overriding their values by external components will disable board operation.
- You must be familiar with signal interconnection design rules. There are many sensitive groups of signals. For example:
  - Ethernet, PCI-Express, SATA, USB and more signals must be routed in differential pairs and by a controlled impedance trace.
  - Audio input must be decoupled from possible sources of carrier board noise.
- Be careful when placing components under the CM-FX6 module. The carrier board interface connector provides 4mm mating height. Bear in mind that there are components on the underside of the CM-FX6. Maximum allowable height for components placed under the CM-FX6 is 1mm.
- Refer to the SB-FX6 carrier board reference design schematics.

8.2 Carrier Board Troubleshooting

- Using grease solvent and a soft brush, clean the contacts of the mating connectors of both the module and the carrier board. Remnants of soldering paste can prevent proper contact. Take care to let the connectors and the module dry entirely before re-applying power – otherwise corrosion may occur.
- Using an oscilloscope, check the voltage levels and quality of the V_ROOT power supply. It should be as specified in section 0. Check that there is no excessive ripple or glitches. First perform the measurements without plugging in the module. Then plug in the module and measure again. Measurement should be performed on the pins of the mating connector.
- Using an oscilloscope, verify that the GND pins of the mating connector are indeed at zero voltage level and that there is no ground bouncing. The module must be plugged in during the test.
- Create a "minimum system" - only power, mating connectors, the module and a serial interface.
- Check if the system starts properly. In system larger than the minimum, possible sources of disturbance could be:
  - Devices improperly driving the local bus

- External pullup/pulldown resistors overriding the module on-board values, or any other component creating the same "overriding" effect
- Faulty power supply

- In order to avoid possible sources of disturbance, it is strongly recommended to start with a minimal system and then to add/activate off-board devices one by one.
- Check for the existence of soldering shorts between pins of mating connectors. Even if the signals are not used on the carrier board, shorting them on the connectors can disable the module operation. An initial check can be performed using a microscope. However, if microscope inspection finds nothing, it is advisable to check using an X-ray, because often solder bridges are deep beneath the connector body. Note that solder shorts are the most probable factor to prevent a module from booting.
- Check possible signal short circuits due to errors in carrier board PCB design or assembly.
- Improper functioning of a customer carrier board can accidentally delete boot-up code from the CM-FX6, or even damage the module hardware permanently. Before every new attempt of activation, check that your module is still functional with CompuLab SB-FX6 carrier board.
- It is recommended to assemble more than one carrier board for prototyping, in order to ease resolution of problems related to specific board assembly.

8.3 Ethernet Magnetics Implementation

8.3.1 Magnetics Selection

Refer to the table below for compatible magnetics. Magnetics listed under the “Recommended Magnetics” section of the table are the magnetics Atheros recommends to use with the AR8033 PHY device. The list of “Qualified Magnetics” contains magnetics verified for proper **functional** operation by CompuLab. Designers should test and qualify all magnetics before using them in an application.

Table 59 Compatible Magnetics

Vendor	P/N	Package
Recommended Magnetics		
Pulse Electronics	H5007	
Qualified Magnetics		
UNE	U50{79}G8-09-B122-B12-BT	Integrated, Dual RJ45
YDS	45F-10202GDD2	Integrated, Dual USB + RJ45

8.3.2 Magnetics Connection

For magnetic modules connection, please refer to the SB-FX6 reference design schematics

8.4 Heat-plate Integration

To be added in a future revision of this document.