SB-T335

Reference Guide

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Table 1 Revision Notes

Date	Description
Sept. 2014	First release

Please check for a newer revision of this manual at the CompuLab web site http://www.compulab.co.il/. Compare the revision notes of the updated manual from the web site with those of the printed or electronic version you have.

1 INTRODUCTION

1.1 About This Document

This document is a part of a set of reference documents providing information necessary to operate and program CompuLab SB-T335.

1.2 Related Documents

For additional information, refer to the documents listed in Table 2.

Table 2 Related Documents

Document	Location
SB-T335 Design Resources	http://www.compulab.com/
CM-T335 Reference Manual	http://www.compulab.com/

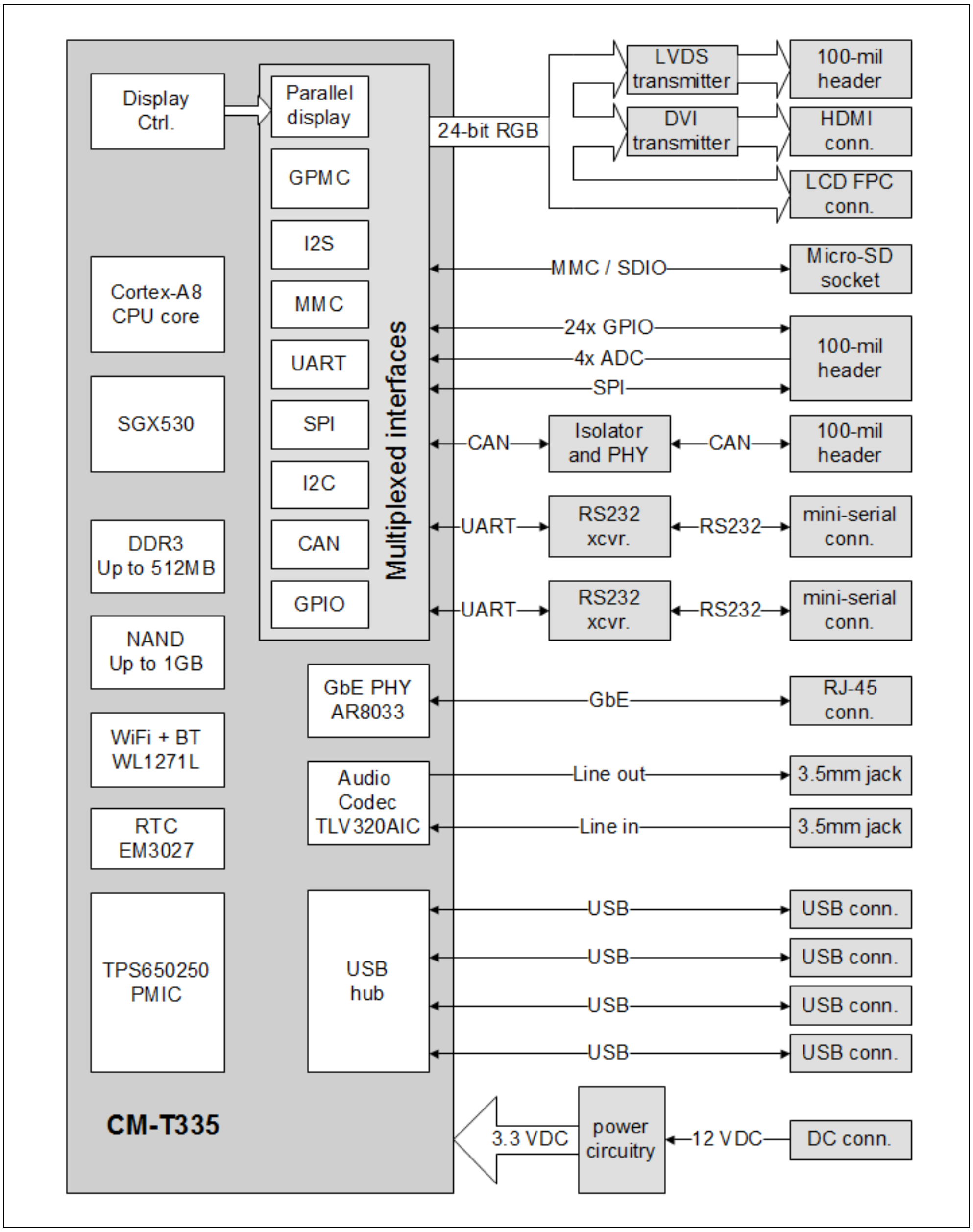
2 OVERVIEW

2.1 Highlights

- Carrier-board designed to support CM-T335 System-on-Module (SoM)
- Implements SBC-T335 Single Board Computer (SBC) when assembled with CM-T335
- DVI-D, LVDS or parallel RGB, up to 1366x768 resolution
- 1000BASE-T Ethernet
- 802.11b/g/n Wi-Fi, Bluetooth 3.0
- 4 USB 2.0 host / 1 USB 2.0 OTG
- 2 RS-232 serial ports
- Analog stereo output, stereo line in and microphone input
- CAN bus
- Micro-SD card socket
- Up to 24 GPIO pins

2.2 Block Diagram

Figure 1 SB-T335 Block Diagram



2.3 Features

The "SB Option" column specifies the P/N code of SB-T335 carrier board required to have the particular feature. The "CM Option" column specifies the P/N code of CM-T335 required to have the particular feature. SBC-T335 feature-set is the combination of features provided by the attached CM-T335 and the features implemented on the SB-T335. To have the particular feature, both the CM and SB options of that feature must be implemented.

"+" sign means that the feature is always available, regardless of P/N code.

Table 3 System and I/O

Feature	Specifications	SB Option	CM Option
CPU RAM Graphics Storage	Refer to CM-T335 specifications		
Display	DVI-D, Up to 1366x768, HDMI connector	+	+
	LVDS, Up to 1366x768, 100-mil header	EVAL	+
	Parallel RGB, Up to 1366x768, FPC connector	EVAL	+
Gigabit Ethernet	1000BASE-T Ethernet. Implemented with the CM-T335 GbE controller. RJ-45 connector with activity LEDs.	+	E
Wi-Fi and Bluetooth	802.11b/g/n implemented with TI WL1271 chipset Bluetooth 3.0 + High Speed (HS) with on-board connector for external antenna Implemented with the CM-T335 on-board wireless module	+	WB
USB	1 OTG USB 2.0 high-speed port, 480 Mbps, micro-AB USB connector	+	U1
	4 host USB 2.0 high-speed ports, 480 Mbps, type-A USB connector	+	U4
Serial Ports	2 RS-232 ports, 2-line RS232 (RX/TX), up to 460 Kbps, mini-serial connector	+	+
Audio I/O	Analog stereo output, analog line-in, 3.5mm jacks Implemented with the CM-T335 audio codec	+	A
CAN	Can bus interface with isolator and driver, 100-mil header	EVAL	+
SDIO	Micro-SD socket	+	+
GPIO	Up to 24 GPIO lines, 100-mil header	+	+
ADC	Up to 4 general purpose ADC inputs, 100-mil header	+	+
RTC	Real Time Clock with an on-board rechargeable Lithium backup battery	+	+

Table 4 Electrical, Mechanical and Environmental Specifications

Supply Voltage	Unregulated 10V to 16V High efficiency switched power supply
Power Consumption	TBD
Dimensions	130mm x 93mm x17mm
MTBF	> 100,000 hours
Operation Temperature (case)	Commercial: 0º to 70º C Extended: -20º to 70º C Industrial: -40º to 85º C See availability note at http://compulab.co.il/products/industrial-temperature-support/
Storage Temperature	-40º to 85º C
Relative Humidity	10% to 90% (operation) 05% to 95% (storage)
Shock	50G / 20 ms
Vibration	20G / 0 - 600 Hz

3 CORE SYSTEM COMPONENTS

3.1 RS-232 Driver/Receiver

Two RS-232 transceivers implemented with TI MAX3243E

- Connected to CM-T335 UART signals
- Operates as an RS-232 PHY with data rate of up to 500kbps
- ESD protection: 15kV HBM, 8kV contact discharge, 15kV air-gap discharge

3.2 LVDS Transmitter

24-bit programmable LVDS DS90C385A transmitter:

- Converts CM-T335 24-bit parallel RGB to LVDS
- Transmits data at 87.5MHz frequency, with throughput of 306.25MBps.
- Supports VGA, SVGA, XGA, SXGA/+ and UXGA
- Compliant with TIA/EIA-644 LVDS standard

3.3 DVI Transmitter

TFP410 digital graphics transmitter:

- Converts CM-T335 24-bit parallel RGB data to DVI interface
- Supports resolutions from VGA to UXGA, with up to 165 MHz pixel rate

3.4 CAN Bus Transceiver

TI ADM3053 signal and power CAN bus transceiver:

- Integrated DC/DC converter, PHY and isolation
- 2.5 kV RMS signal and power isolation
- Connected to CM-T335 CAN Bus interface

3.5 GPIO Controller

A CAT9555 16-bit I^{2}C I/O port controller:

- Controls 16 on-board GPIO lines.
- I^{2}C serial interface, up to 400kHz
- I^{2}C address: 26h
- Individual pin I/O configuration

3.6 RTC Backup Battery

The SB-T335 is equipped with an ML1220 backup battery in order to maintain the CM-T335 RTC whenever main power is not present. The battery capacity is 18mAh, with nominal voltage of 3V.

3.7 DC Power supply

SB-T335 power supply circuitry receives a +12V supply from the power jack.

The power supply circuit consists of filtering components and voltage converting sub-circuits, meant to supply 5V and 3.3V to the on-board components and to the CM-T335 SoM.

SW1 power button turns the device on and off: short press to turn on, short press to turn off by an interrupt signal (software off), or long press for hardware off.

4 INTERFACES AND CONNECTORS

4.1 Display Interface

4.1.1 DVI

SB-T335 features DVI-D display output, with an HDMI type-A female connector.

TFP410 digital graphics transmitter receives a 24-bit display data from CM-T335 and converts it to DVI-D video interface.

4.1.2 LVDS

LVDS interface is derived from an on-board DS90C385A transmitter, which converts the 24-bit display data from the CM-T335.

LVDS interface is available via the 16-pin 100-mil header P6.

Along with LVDS signal, P6 header includes two backlight supply pins: WLD_OUT for anode connection, and WLD_CAT for cathode connection. The voltage levels of the above pins meet the needs of a typical LED backlight configuration of 6 serially connected LEDs, with up to 3.6V each, i.e. 21.6V maximum total voltage. The power supply of the backlight is controlled by PWM0, a configurable Pulse Width Modulation signal. Note that PWM0 signal is derived from the CM-T335 and can be accessed via P6 header.

Header P6 is available only with 'EVAL' option of the SB-T335. The pinout of the P6 header is described in Table 5.

Table 5 LVDS connector pin-out (P6)

Pin #	Signal Name	Type	Description	Availability
P6-1	WLD_OUT	PWR	Backlight anode	Available with 'EVAL' option
P6-2	WLD_CAT	PWR	Backlight cathode	Available with 'EVAL' option
P6-3	LVDS_P0	O	LVDS 0 +	Available with 'EVAL' option
P6-4	LVDS_N0	O	LVDS 0 -	Available with 'EVAL' option
P6-5	LVDS_P1	O	LVDS 1 +	Available with 'EVAL' option
P6-6	LVDS_N1	O	LVDS 1 -	Available with 'EVAL' option
P6-7	LVDS_P2	O	LVDS 2 +	Available with 'EVAL' option
P6-8	LVDS_N2	O	LVDS 2 -	Available with 'EVAL' option
P6-9	eGPIO5	IO	GPIO LVDS control	Available with 'EVAL' option
P6-10	PWM0	IO	PWM0	Available with 'EVAL' option
P6-11	LVDS_P3	O	LVDS 3 +	Available with 'EVAL' option
P6-12	LVDS_N3	O	LVDS 3 -	Available with 'EVAL' option
P6-13	VCM	PWR	3.3V power output	Available with 'EVAL' option
P6-14	GND	PWR	Ground	Available with 'EVAL' option
P6-15	LVDS_CLKP	O	LVDS Clock +	Available with 'EVAL' option
P6-16	LVDS_CLKN	O	LVDS Clock -	Available with 'EVAL' option

4.1.3 LCD Panel Connector

SB-T335 with 'EVAL' option is equipped with a 50-pin 0.5mm LCD panel connector P5.

Connector P5 is located on the bottom side of SB-T335 and includes 24 parallel RGB signals, an SPI bus, an I^2C bus, 4 analog touchscreen inputs, backlight supply pins and several other control and data pins. For detailed pinout of connector P5 see Table 6.

Table 6 LCD panel connector pin-out (P5)

Pin #	Signal Name	Type	Description	Availability
P5-1	WLD_OUT	PWR	Backlight anode	Available with 'EVAL' option
P5-2	WLD_CAT	PWR	Backlight cathode	Available with 'EVAL' option
P5-3	VCM	PWR	3.3V power output	Available with 'EVAL' option
P5-4	I2C0_SCL	IO	I^2C 0 Clock	Available with 'EVAL' option
P5-5	I2C0_SDA	IO	I^2C 0 Data	Available with 'EVAL' option
P5-6	VCM	PWR	3.3V power output	Available with 'EVAL' option
P5-7	GMPC_CS2	I	Touch screen interrupt	Available with 'EVAL' option
P5-8	NC	-	Not Connected	Available with 'EVAL' option
P5-9	GND	PWR	Ground	Available with 'EVAL' option
P5-10	LCD_DATA4	O	Parallel RGB signal – R7	Available with 'EVAL' option
P5-11	LCD_DATA3	O	Parallel RGB signal – R6	Available with 'EVAL' option
P5-12	LCD_DATA2	O	Parallel RGB signal – R5	Available with 'EVAL' option
P5-13	LCD_DATA1	O	Parallel RGB signal – R4	Available with 'EVAL' option
P5-14	LCD_DATA0	O	Parallel RGB signal – R3	Available with 'EVAL' option
P5-15	LCD_DATA16	O	Parallel RGB signal – R2	Available with 'EVAL' option
P5-16	LCD_VSYNC	O	LCD Vertical Sync	Available with 'EVAL' option
P5-17	LCD_HSYNC	O	LCD Horizontal Sync	Available with 'EVAL' option
P5-18	GND	PWR	Ground	Available with 'EVAL' option
P5-19	SPI_SCLK	IO	SPI Clock	Available with 'EVAL' option
P5-20	SPI_CS	O	SPI Chip Select	Available with 'EVAL' option
P5-21	SPI_MOSI	O	SPI MOSI	Available with 'EVAL' option
P5-22	SPI_MISO	I	SPI MISO	Available with 'EVAL' option
P5-23	LCD_BIAS_EN	O	LCD Bias Enable	Available with 'EVAL' option
P5-24	GND	PWR	Ground	Available with 'EVAL' option
P5-25	LCD_PCLK	O	LCD Pixel Clock	Available with 'EVAL' option
P5-26	GND	PWR	Ground	Available with 'EVAL' option
P5-27	LCD_DATA18	O	Parallel RGB signal – R1	Available with 'EVAL' option
P5-28	LCD_DATA21	O	Parallel RGB signal – R0	Available with 'EVAL' option
P5-29	LCD_DATA10	O	Parallel RGB signal – G7	Available with 'EVAL' option
P5-30	LCD_DATA9	O	Parallel RGB signal – G6	Available with 'EVAL' option
P5-31	LCD_DATA8	O	Parallel RGB signal – G5	Available with 'EVAL' option
P5-32	LCD_DATA7	O	Parallel RGB signal – G4	Available with 'EVAL' option
P5-33	LCD_DATA6	O	Parallel RGB signal – G3	Available with 'EVAL' option
P5-34	LCD_DATA5	O	Parallel RGB signal – G2	Available with 'EVAL' option
P5-35	LCD_DATA19	O	Parallel RGB signal – G1	Available with 'EVAL' option
P5-36	LCD_DATA22	O	Parallel RGB signal – G0	Available with 'EVAL' option
P5-37	LCD_DATA15	O	Parallel RGB signal – B7	Available with 'EVAL' option
P5-38	LCD_DATA14	O	Parallel RGB signal – B6	Available with 'EVAL' option
P5-39	LCD_DATA13	O	Parallel RGB signal – B5	Available with 'EVAL' option
P5-40	LCD_DATA12	O	Parallel RGB signal – B4	Available with 'EVAL' option
P5-41	LCD_DATA11	O	Parallel RGB signal – B3	Available with 'EVAL' option
P5-42	LCD_DATA17	O	Parallel RGB signal – B2	Available with 'EVAL' option
P5-43	LCD_DATA20	O	Parallel RGB signal – B1	Available with 'EVAL' option
P5-44	LCD_DATA23	O	Parallel RGB signal – B0	Available with 'EVAL' option
P5-45	PARDISP_RST	O	Display Reset	Available with 'EVAL' option
P5-46	GND	PWR	Ground	Available with 'EVAL' option
P5-47	AIN2	AI	Analog touchscreen input – YU	Available with 'EVAL' option
P5-48	AIN3	AI	Analog touchscreen input – YD	Available with 'EVAL' option
P5-49	AIN0	AI	Analog touchscreen input – XL	Available with 'EVAL' option
P5-50	AIN1	AI	Analog touchscreen input – XR	Available with 'EVAL' option

4.2 Ethernet

4.2.1 Ethernet via RJ45

The CM-T335 Ethernet interface is available via the on-board RJ-45 connector P2.

4.2.2 RGMII

In case SB-T335 is assembled with CM-T335 without the 'E' configuration option, CM-T335 RGMII signals are available via the 16-pin 100-mil header P24.

Table 7 RGMII header pin-out (P24)

Pin #	Signal Name	Type	Description	Availability
P24-1	5V	PWR	5.0V power output	Always available
P24-2	VCM	PWR	3.3V power output	Always available
P24-3	RGMII_RXD0	I	RGMII RX 0	CM-T335 without 'E' option
P24-4	RGMII_TXEN	O	RGMII TX Enable	CM-T335 without 'E' option
P24-5	RGMII_RXD1	I	RGMII RX 1	CM-T335 without 'E' option
P24-6	RGMII_TXD0	O	RGMII TX 0	CM-T335 without 'E' option
P24-7	RGMII_RXD2	I	RGMII RX 2	CM-T335 without 'E' option
P24-8	RGMII_TXD1	O	RGMII TX 1	CM-T335 without 'E' option
P24-9	RGMII_RXD3	I	RGMII RX 3	CM-T335 without 'E' option
P24-10	RGMII_TXD2	O	RGMII TX 2	CM-T335 without 'E' option
P24-11	RGMII_RXDV	I	RGMII RX Control	CM-T335 without 'E' option
P24-12	RGMII_TXD3	O	RGMII TX 3	CM-T335 without 'E' option
P24-13	MDIO_CLK	IO	MDIO Clock	CM-T335 without 'E' option
P24-14	MDIO_DATA	IO	MDIO Data	CM-T335 without 'E' option
P24-15	RGMII_RXCLK	I	RGMII RX Clock	CM-T335 without 'E' option
P24-16	RGMII_TXCLK	O	RGMII TX Clock	CM-T335 without 'E' option

NOTE: Some of P24 pins are multifunctional. For more functions and availability refer to Chapter 4.10: Multifunctional Pin Headers.

4.3 Wi-Fi and Bluetooth

Wi-Fi 802.11b/g/n and Bluetooth 3.0 wireless interfaces are implemented with CM-T335 SoM. A single 2.4GHz antenna needs to be connected to the CM-T335 U.FL connector for proper Wi-Fi and Bluetooth communication. No Wi-Fi or Bluetooth functions are implemented on-board SB-T335.

4.4 USB

A USB hub is assembled on CM-T335 only with 'U4' configuration option. For more information refer to CM-T335 documentation.

In case SB-T335 is assembled with CM-T335 with 'U4' configuration option, four USB2.0 host ports are available through standard USB type-A connectors P25, P26, P27 and P28. In case SB-T335 is assembled with CM-T335 without the 'U4' configuration option, a single USB port is available via the OTG USB 2.0 connector P19.

4.5 RS232

SB-T335 is equipped with two RS-232 interfaces available via ultra-mini 8-pin connectors.

The pinout of RS232 ultra-mini connectors is detailed in Table 8, according to the pin numbers described in Figure 2.

Figure 2 RS232 Connectors

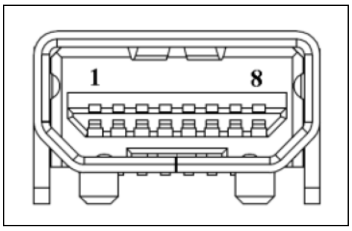


Table 8 RS232 connector pin-out

Pin #	Signal Name	Type	Description	Availability
1	RS232_TXD	O	RS232 Data Transmit	Always available
2	NC	-	Not Connected	Always available
3	RS232_RXD	I	RS232 Data Receive	Always available
4	NC	-	Not Connected	Always available
5	NC	-	Not Connected	Always available
6	NC	-	Not Connected	Always available
7	NC	-	Not Connected	Always available
8	GND	PWR	Ground	Always available

4.6 Audio

The audio I/O of SB-T335 is available only when a CM-T335 with the 'A' configuration option is assembled.

SB-T335 provides analog stereo line-in on 3.5mm jack P29 and analog stereo output on 3.5mm jack P30. Microphone input and bias lines are available through 100-mil connector P13.

Audio connections are detailed in Table 9.

Table 9 Audio I/O connectors pin-out

Connection	Signal	Type	Availability
P29 (audio input)			
Tip	Analog audio in, left channel / mono	AO	CM-T335 with ‘A’ option
Ring	Analog audio in, right channel / mono	AO	CM-T335 with ‘A’ option
Sleeve	GND	PWR	Always available
P30 (audio output)			
Tip	Analog audio out, left channel	AI	CM-T335 with ‘A’ option
Ring	Analog audio out, right channel	AI	CM-T335 with ‘A’ option
Sleeve	GND	PWR	Always available
P30 (microphone)			
P13 - 1	Microphone bias	AO	CM-T335 with ‘A’ option
P13 - 2	Microphone input	AI	CM-T335 with ‘A’ option

4.7 SDIO/MMC

Four SDIO/MMC data signals along with clock and control signals are routed from CM-T335 to the SB-T335 micro-SD socket P23.

This micro-SD socket supports data transfer rate of up to 192Mbps (24MBps), in High-Speed SD mode, using 4-bit data transfer.

NOTE: Additional SDIO/MMC signals are accessible via on-board 100-mil headers. For more information refer to Chapter 4.10: Multifunctional Pin Headers.

4.8 CAN-Bus

SB-T335 provides an 8-pin 100-mil header for CAN bus connectivity.

CAN bus power can be provided or supplied externally via the CAN-VCC pin. Power supply source is configured with jumper E1. When E1 is assembled, SB-T335 supplies power to the CAN bus; when jumper E1 is not assembled, the CAN bus controller power is fed from the bus.

Table 10 CAN Bus header pin-out (P14)

Pin #	Signal Name	Type	Description	Availability
P14 - 1	CAN_GND	PWR	Isolated CAN bus Ground	Always available
P14 - 2	CAN_VCC	PWR	Isolated CAN bus power input/output	Always available
P14 - 3	CAN_H	IO	CAN bus High	Always available
P14 - 4	NC	-	Not Connected	Always available
P14 - 5	CAN_L	IO	CAN bus Low	Always available
P14 - 6	NC	-	Not Connected	Always available
P14 - 7	GND	PWR	Ground	Always available
P14 - 8	NC	-	Not Connected	Always available

4.9 SPI

SPI bus can be accessed via the LCD connector P5 (see P5 pinout), or through the GMPC/SPI/multifunctional 100-mil 34-pin header P20. Two separate devices can be connected to SPI bus via header P20, since two chip-select (CS) signals are available.

The SPI signals on header P20 are detailed in Table 11.

Table 11 SPI Bus connector pin-out (part of P20)

Pin #	Signal Name	Type	Description	Availability
P20 - 23	SPI0_DO_SB	O	SPI MOSI	Always available
P20 - 25	SPI0_CS0_SB	O	SPI Chip Select 0	Always available
P20 - 27	SPI0_DI_SB	I	SPI MISO	Always available
P20 - 29	SPI0_CS1_SB	O	SPI Chip Select 1	Always available
P20 - 33	SPI_SCLK_SB	O	SPI Clock	Always available

NOTE: Table 11 describes only the SPI functionality of a part of P20 header pins. For complete functionality and full pin description see Chapter 4.10: Multifunctional Pin Headers

4.10 Multifunctional Pin Headers

SB-T335 includes two multifunctional pin headers: P20 and P24. Functionality of these headers is partially described in previous chapters, according to the specific functions.

P20 – GPMC / SPI / Multifunctional

Header P20 is a 100-mil, 34-pin, GMPC/SPI/Multifunctional header. The functionalities of P20 pins are detailed in Table 12.

It table 12, ALT0 is the primary mode of each terminal. Any mode can be selected between ALT0 to ALT7. Some modes match to a functional configuration, while others, identified by blank ALT cell in Table 12, coincident to no functional configuration.

Table 12 P20 Header Pinout

Pin #	ALT 0	ALT 1	ALT 2	ALT 3	ALT 4	ALT 5	ALT 6	ALT 7
1	GPMC_WPN	GMII2_RXER	GPMC_CSN5	RMII2_RXER	MMC2_SDCD_MUX0	PR1_MII1_TXEN	UART4_TXD_MUX2	GPIO0(31)
2	AIN4							
3	GPMC_CSN3			MMC2_CMD_MUX0	PR1_MII0_CRS_MUX0	PR1_MDIO_DATA	EMU4_MUX0	GPIO2(0)
4	AIN5							
5	GPMC_CSN2	GPMC_BE1N_MUX1	MMC1_CMD_MUX0	PR1_EDIO_DATA_IN7_MUX0	PR1_EDIO_DATA_OUT7_MUX0	PR1_PRU1_PRU_R30[13]	PR1_PRU1_PRU_R31[13]	GPIO1(31)
6	AIN6							
7	GPMC_CSN1	GPMC_CLK_MUX1	MMC1_CLK_MUX0	PR1_EDIO_DATA_IN6_MUX0	PR1_EDIO_DATA_OUT6_MUX0	PR1_PRU1_PRU_R30[12]	PR1_PRU1_PRU_R31[12]	GPIO1(30)
8	AIN7							
9	GPMC_BE1N_MUX0	GMII2_COL	GPMC_CSN6	MMC2_DAT3_MUX0	GPMC_DIR	PR1_MII1_RXLINK	MCASP0_ACLKR_MUX3	GPIO1(28)
10	GPMC_AD0	MMC1_DAT0_MUX2						GPIO1(0)
11	GPMC_CLK_MUX0	LCD_MEMORY_CLK_MUX0	GPMC_WAIT1	MMC2_CLK_MUX0	PR1_MII1_CRS_MUX0	PR1_MDIO_MDCLK	MCASP0_FSR_MUX3	GPIO2(1)
12	GPMC_AD1	MMC1_DAT1_MUX2						GPIO1(1)
13	GPMC_BE0N_CLE		TIMER5_MUX3					GPIO2(5)
14	GPMC_AD2	MMC1_DAT2_MUX2						GPIO1(2)
15	GPMC_WAIT0	GMII2_CRS	GPMC_CSN4	RMII2_CRS_DV	MMC1_SDCD_MUX0	PR1_MII1_COL	UART4_RXD_MUX2	GPIO0(30)
16	GPMC_AD3	MMC1_DAT3_MUX2						GPIO1(3)
17	GPMC_WEN		TIMER6_MUX3					GPIO2(4)
18	GPMC_AD4	MMC1_DAT4_MUX2						GPIO1(4)
19	LCD_PCLK	GPMC_A10_MUX1	PR1_MII0_CRS_MUX1	PR1_EDIO_DATA_IN4	PR1_EDIO_DATA_OUT4	PR1_PRU1_PRU_R30[10]	PR1_PRU1_PRU_R31[10]	GPIO2(24)
20	GPMC_AD5	MMC1_DAT5_MUX2						GPIO1(5)
21	GPMC_ADVN_ALE		TIMER4_MUX3					GPIO2(2)
22	GPMC_AD6	MMC1_DAT6_MUX2						GPIO1(6)
23	SPI0_D0	UART2_TXD_MUX3	I2C2_SCL_MUX2	EHRPWM0B_MUX1	PR1_UART0_RTS_N_MUX0	PR1_EDIO_LATCH_IN	EMU3_MUX1	GPIO0(3)
24	GPMC_AD7	MMC1_DAT7_MUX2						GPIO1(7)
25	SPI0_CS0	MMC2_SDWP_MUX0	I2C1_SCL_MUX3	EHRPWM0_SYNCI_MUX1	PR1_UART0_TXD_MUX0	PR1_EDIO_DATA_IN1	PR1_EDIO_DATA_OUT1	GPIO0(5)
26	NC							

27	SPI0_D1	MMC1_SDWP_MUX0	I2C1_SDA_MUX3	EHRPWM0_TRIPZONE_INPUT_MUX1	PR1_UART0_RXD_MUX0	PR1_EDIO_DATA_IN0	PR1_EDIO_DATA_OUT0	GPIO0(4)
28	NC							
29	SPI0_CS1	UART3_RXD_MUX1	ECAP1_IN_PWM1_OUT_MUX0	MMC0_POW_MUX1	XDMA_EVENT_INTR2_MUX1	MMC0_SDCD_MUX0	EMU4_MUX1	GPIO0(6)
30	VCM (3.3V)							
31	NC							
32	5V							
33	SPI0_SCLK	UART2_RXD_MUX3	I2C2_SDA_MUX2	EHRPWM0A_MUX1	PR1_UART0_CTS_N_MUX0	PR1_EDIO_SOF	EMU2_MUX1	GPIO0(2)
34	GND							

NOTE: Pin function selection is controlled by software. Only a single function can be used at a time. For additional details, refer to the CM-T335 Reference Guide and to the AM335 SoC Reference Manual.

P24 – RGMII / Multifunctional

Header P24 is a 100-mil, 16-pin, RGMII/Multifunctional header. The functionalities of the P24 pins are detailed in Table 13.

In table 13, ALT0 is the primary mode of each terminal. Any mode can be selected between ALT0 to ALT7. Some modes match to a functional configuration, while others, identified by blank ALT cell in Table 13, coincident to no functional configuration.

Table 13 P24 Header Pinout

Pin #	ALT 0	ALT 1	ALT 2	ALT 3	ALT 4	ALT 5	ALT 6	ALT 7
1	5V							
2	VCM (3.3V)							
3	GMII1_RXD0	RMII1_RXD0	RGMII1_RD0	MCASP1_AHCLKX_MUX0	MCASP1_AHCLKR_MUX0	MCASP1_ACLKR_MUX1	MCASP0_AXR3_MUX4	GPIO2(21)
4	GMII1_TXEN	RMII1_TXEN	RGMII1_TCTL	TIMER4_MUX0	MCASP1_AXR0_MUX1	EQEP0_INDEX_MUX1	MMC2_CMD_MUX2	GPIO3(3)
5	GMII1_RXD1	RMII1_RXD1	RGMII1_RD1	MCASP1_AXR3_MUX0	MCASP1_FSR_MUX0	EQEP0_STROBE_MUX1	MMC2_CLK_MUX2	GPIO2(20)
6	GMII1_TXD0	RMII1_TXD0	RGMII1_TD0	MCASP1_AXR2_MUX0	MCASP1_ACLKR_MUX0	EQEP0B_IN_MUX1	MMC1_CLK_MUX1	GPIO0(28)
7	GMII1_RXD2	UART3_TXD_MUX0	RGMII1_RD2	MMC0_DAT4	MMC1_DAT3_MUX1	UART1_RIN_MUX0	MCASP0_AXR1_MUX2	GPIO2(19)
8	GMII1_TXD1	RMII1_TXD1	RGMII1_TD1	MCASP1_FSR_MUX1	MCASP1_AXR1_MUX0	EQEP0A_IN_MUX1	MMC1_CMD_MUX1	GPIO0(21)
9	GMII1_RXD3	UART3_RXD_MUX0	RGMII1_RD3	MMC0_DAT5	MMC1_DAT2_MUX1	UART1_DTRN_MUX0	MCASP0_AXR0_MUX2	GPIO2(18)
10	GMII1_TXD2	DCAN0_RX_MUX0	RGMII1_TD2	UART4_TXD_MUX0	MCASP1_AXR0_MUX0	MMC2_DAT2_MUX2	MCASP0_AHCLKX_MUX2	GPIO0(17)
11	GMII1_RXDV	LCD_MEMORY_CLK_MUX1	RGMII1_RCTL	UART5_TXD_MUX1	MCASP1_ACLKX_MUX0	MMC2_DAT0_MUX2	MCASP0_ACLKR_MUX2	GPIO3(4)
12	GMII1_TXD3	DCAN0_TX_MUX0	RGMII1_TD3	UART4_RXD_MUX0	MCASP1_FSX_MUX0	MMC2_DAT1_MUX2	MCASP0_FSR_MUX2	GPIO0(16)
13	MDIO_CLK	TIMER5_MUX2	UART5_TXD_MUX3	UART3_RTSN_MUX2	MMC0_SDWP_MUX2	MMC1_CLK_MUX2	MMC2_CLK_MUX1	GPIO0(1)
14	MDIO_DATA	TIMER6_MUX2	UART5_RXD_MUX3	UART3_CTSN_MUX2	MMC0_SDCD_MUX2	MMC1_CMD_MUX2	MMC2_CMD_MUX1	GPIO0(0)
15	GMII1_RXCLK	UART2_TXD_MUX0	RGMII1_RCLK	MMC0_DAT6	MMC1_DAT1_MUX1	UART1_DSRN_MUX0	MCASP0_FSX_MUX2	GPIO3(10)
16	GMII1_TXCLK	UART2_RXD_MUX0	RGMII1_TCLK	MMC0_DAT7	MMC1_DAT0_MUX1	UART1_DCDN_MUX0	MCASP0_ACLKX_MUX2	GPIO3(9)

NOTE: Pin function selection is controlled by software. Only a single function can be used at a time. For additional details, refer to the CM-T335 Reference Guide and to the AM335 SoC Reference Manual.

4.11 CM-T335 SoM Interface

The SB-T335 is equipped with a standard 204-pin SODIMM socket, in order to host the CM-T335 SoM. Connector pin-out is detailed in Table 14.

Table 14 Connector Pinout

Pin #	CM-T335 Signal Name	AM335x Signal Name	Type	Description
1	VIN		PWR	Main power supply, 5V typ.
2	NC			Not connected
3	GPMC_WE#	GPMC_WEn	O	GPMC Write Enable (active low)
4	NC			Not connected
5	GPMC_WAIT0	GPMC_WAIT0	I	Ext. wait signal for access time control (PU)
6	AIN2	AIN2	AIO	GP analog input/output / touch screen input
7	nRESET	RTC_PWRONRSTN	I	Global cold reset (active low)
8	VIN		PWR	Main power supply, 5V typ.
9	NC			Not connected
10	AIN0	AIN0	AIO	GP analog input/output / touch screen input
11	AIN5	AIN5	AI	GP analog input / touch screen input
12	AIN4	AIN4	AIO	GP analog input/output / touch screen input
13	NC			Not connected
14	AIN3	AIN3	AIO	GP analog input/output / touch screen input
15	WARMRST#	nRESETIN_OUT	I	Global warm reset (active low)
16	AIN7	AIN7	AI	GP analog input / touch screen input
17	GND			Digital ground
18	AIN6	AIN6	AI	GP analog input / touch screen input
19	NC			Not connected
20	AIN1	AIN1	AIO	GP analog input/output / touch screen input
21	GPMC_CLE	GPMC_BE0n_CLE	O	Command Line Enable for NAND protocol
22	NC			Not connected
23	GPMC_AD1	GPMC_AD1	IO	GPMC DATA 1
24	GND			Digital ground
25	NC			Not connected
26	LCD_DATA15	LCD_DATA15	O	LCD data bus
27	NC			Not connected
28	LCD_DATA5	LCD_DATA5	O	LCD data bus
29	NC			Not connected
30	LCD_DATA7	LCD_DATA7	O	LCD data bus
31	NC			Not connected
32	LCD_DATA6	LCD_DATA6	O	LCD data bus
33	VIN		PWR	Main power supply, 5V typ.
34	NC			Not connected
35	NC			Not connected
36	NC			Not connected
37	NC			Not connected
38	NC			Not connected
39	LCD_DATA11	LCD_DATA11	O	LCD data bus
40	VIN			Main power supply, 5V typ.
41	LCD_DATA14	LCD_DATA14	O	LCD data bus
42	NC			Not connected
43	LCD_DATA13	LCD_DATA13	O	LCD data bus
44	LCD_DATA2	LCD_DATA2	O	LCD data bus
45	LCD_DATA0	LCD_DATA0	O	LCD data bus
46	LCD_DATA10	LCD_DATA10	O	LCD data bus
47	LCD_DATA3	LCD_DATA3	O	LCD data bus
48	LCD_DATA12	LCD_DATA12	O	LCD data bus
49	GND			Digital ground
50	LCD_DATA9	LCD_DATA9	O	LCD data bus

51	NC			Not connected
52	LCD_DATA8	LCD_DATA8	O	LCD data bus
53	LCD_DATA1	LCD_DATA1	O	LCD data bus
54	LCD_DATA4	LCD_DATA4	O	LCD data bus
55	NC			Not connected
56	GND			Digital ground
57	NC			Not connected
58	LCD_VSYNC	LCD_VSYNC	O	LCD Vertical Sync
59	EXT_WAKEUP	EXT_WAKEUP	I	External wake-up input
60	LCD_HSYNC	LCD_HSYNC	O	LCD Horizontal Sync
61	NC			Not connected
62	NC			Not connected
63	GPMC_AD0	GPMC_AD0	IO	GPMC DATA 0
64	NC			Not connected
65	VIN		PWR	Main power supply, 5V typ.
66	NC			Not connected
67	GPMC_RE#	GPMC_OEn_REn	O	GPMC Read Enable (active low)
68	LCD_DATA21	LCD_DATA21	O	LCD data bus
69	LCD_PCLK	LCD_PCLK	O	LCD Pixel Clock
70	LCD_DATA19	LCD_DATA19	O	LCD data bus
71	LCD_BIAS_EN	LCD_AC_BIAS_EN	O	LCD AC bias enable chip select
72	VIN		PWR	Main power supply, 5V typ.
73	GPMC_ALE	GPMC_ADVn_ALE	O	Add. Latch Enable for NAND/NOR
74	LCD_DATA20	LCD_DATA20	O	LCD data bus
75	GPMC_AD3	GPMC_AD3	IO	GPMC DATA 3
76	LCD_DATA18	LCD_DATA18	O	LCD data bus
77	GPMC_AD4	GPMC_AD4	IO	GPMC DATA 4
78	GPMC_AD5	GPMC_AD5	IO	GPMC DATA 5
79	GPMC_CS1	GPMC_CSn1	O	GPMC Chip Select 1 (active low)
80	GPMC_AD2		IO	GPMC DATA 2
81	GND			Digital ground
82	GPMC_AD6	GPMC_AD6	IO	GPMC DATA 6
83	LCD_DATA23	LCD_DATA23	O	LCD data bus
84	GPMC_AD7	GPMC_AD7	IO	GPMC DATA 7
85	LCD_DATA22	LCD_DATA22	O	LCD data bus
86	GPMC_CS2	GPMC_CSn2	O	GPMC Chip Select 2 (active low)
87	GPMC_CLK	GPMC_CLK	O	GPMC synchronous mode clock
88	GND			Digital ground
89	LCD_DATA17	LCD_DATA17	O	LCD data bus
90	GPMCCS3_GPIO2_0	GPMC_CSn3	O	GPMC Chip Select 3, LED (active low)
91	LCD_DATA16	LCD_DATA16	O	LCD data bus
92	GPMC_WP#	GPMC_WPn	O	GPMC Write Protect (active low)
93	GPMC_BEN1	GPMC_BE1n	O	GPMC Byte Enable 1
94	USB_CHARGEN_OUT	USB0_CE	AO	USB0 Active high Charger Enable output
95	MMC0_DAT1	MMC0_DAT1	IO	MMC/SD/SDIO Data bus
96	PWM0	ECAP0_IN_PWM0_OUT	IO	Auxiliary PWM0 output
97	VIN		PWR	Main power supply, 5V typ.
98	USB0_HUB_VBUS	USB0_VBUS	PWR	USB power supply, regulated by the SoC
99	MMC0_CLK	MMC0_CLK	IO	MMC/SD/SDIO Command
100	VIN		PWR	Main power supply, 5V typ.
101	MMC0_DAT0	MMC0_DAT0	IO	MMC/SD/SDIO Data bus
102	MMC0_DAT3	MMC0_DAT3	IO	MMC/SD/SDIO Data bus
103	MMC0_DAT2	MMC0_DAT2	IO	MMC/SD/SDIO Data bus
104	RGMII_RXCLK	RGMII1_RCLK	I	RGMII Receive Clock
105	RGMII_RXD0	RGMII1_RD0	I	RGMII Receive Data bit 0
106	RGMII_RXD1	RGMII1_RD1	I	RGMII Receive Data bit 1
107	RGMII_RXD2	RGMII1_RD2	I	RGMII Receive Data bit 2
108	ETH_LINK-LED_10_100		O	Ethernet 10/100 Base-T LED (active high)
109	RGMII_TXD3	RGMII1_TD3		RGMII Transmit Data bit 3
110	ETH_LINK-LED_1000		O	Ethernet 1000 Base-T LED (active high)
111	VIN		PWR	Main power supply, 5V typ.
112	ETH_LED_ACT		O	Ethernet blinking LED (active high)
113	RGMII_TXCLK	RGMII1_TCLK	O	RGMII Transmit Clock
114	RGMII_TXD0	RGMII1_TD0	O	RGMII Transmit Data bit 0
115	RGMII_TXD1	RGMII1_TD1	O	RGMII Transmit Data bit 1
116	ETH_MDI3-		IO	Ethernet MDI N3
117	RGMII_TXD2	RGMII1_TD2	O	RGMII Transmit Data bit 2

118	ETH_MDI3+		IO	Ethernet MDI P3
119	RGMII_TXEN	RGMII1_TCTL	O	RGMII Transmit Control
120	VIN		PWR	Main power supply, 5V typ.
121	RGMII_RXD3	RGMII1_RD3		RGMII Receive Data bit 3
122	ETH_MDI2-		IO	Ethernet MDI N2
123	MDIO_CLK	MDIO_CLK	O	MDIO Clock
124	ETH_MDI2+		IO	Ethernet MDI P2
125	RGMII_RXDV	RGMII1_RCTL	I	RGMII Receive Control
126	MDIO_DATA	MDIO_DATA	IO	MDIO Data
127	GND			Digital ground
128	ETH_MDI1-		IO	Ethernet MDI N1
129	EMU0	EMU0	O	Ethernet PHY reset
130	ETH_MDI1+		IO	Ethernet MDI P1
131	EMU1	EMU1	O	WLAN interrupt request
132	GND			Digital ground
133	EXTINTN	EXTINTN	I	External Interrupt (active low)
134	ETH_MDI0-		IO	Ethernet MDI N0
135	AUDIO_OUT_L		AO	Analog audio output L
136	ETH_MDI0+		IO	Ethernet MDI P0
137	AUDIO_OUT_R		AO	Analog audio output L
138	UART0CTSn_I2C1D	I2C1_SDA/UART0_CTSn	IO	I2C Data / UART0 Clear To Send
139	UART0RTSn_I2C1CLK	I2C1_SCL/UART0_RTSN	IO	I2C Clock / UART0 Request To Send
140	TCK	TCK	I	JTAG TCK
141	MCASP_1AXR2	MCASP1_AXR2	IO	McASP Serial Data
142	TDO	TDO	O	JTAG TDO
143	VIN		PWR	Main power supply, 5V typ.
144	I2C0_SCL	I2C0_SCL	IO	I2C 0 Clock
145	MIC_BIAS		AI	Analog microphone bias
146	2C0_SDA	2C0_SDA	IO	I2C 0 Data
147	MIC_IN		AI	Analog microphone input
148	VIN		PWR	Main power supply, 5V typ.
149	TDI	TDI	I	JTAG TDI
150	VDD_RTC_BACK		PWR	Backup power supply for RTC
151	RS232_RXD		I	RS232 RXD
152	EEPROM_WP		I	EEPROM Write Protect
153	RS232_CTSn		I	RS232 CTS (active low)
154	TRSTN	TRSTN	I	JTAG Test Reset (active low)
155	MMC0_CMD	MMC0_CMD	IO	MMC/SD/SDIO Command
156	RS232_TXD		O	RS232 TXD
157	MCASP_1AXR3	MCASP1_AXR3	IO	McASP Serial Data
158	RS232_PHYIND		O	RS232 PHY indicator, low active ('Z' conf.)
159	GND			Digital ground
160	RS232_RTSn		O	RS232 RTS
161	USB1_DN		IO	USB1 Data N
162	ETHCM_SB		O	Ethernet PHY indicator, high active
163	USB1_DP		IO	USB1 Data P
164	GND			Digital ground
165	UART1_RXD_SB	UART1_RXD	I	UART 1 RX (not available on Z conf.)
166	AUDIO_IN_R/MONO		AI	Audio line in channel R / mono
167	USB2_DN		IO	USB2 Data N
168	AUDIO_IN_L/MONO		AI	Audio line in channel L / mono
169	USB2_DP		IO	USB2 Data P
170	UART0_RXD		I	UART 0 RX
171	TMS	TMS	I	JTAG TMS
172	UART0_TXD		O	UART 0 TX
173	USB3_DN		IO	USB3 Data N
174	SPI0_DI_SB	SPI0_D1	IO	SPI D1 (not available on WB conf.)
175	USB3_DP		IO	USB3 Data P
176	SPI0_CS0_SB	SPI0_CS0		SPI CS0
177	VIN		PWR	Main power supply, 5V typ.
178	NC			Not connected
179	USB4_DN		IO	USB4 Data N
180	VIN		PWR	Main power supply, 5V typ.
181	USB4_DP		IO	USB4 Data P
182	SPI0_CS1_SB	SPI0_CS1_SB		SPI CS1 (not available on WB conf.)
183	USB1_CPEN		I	USB1 Power Enable (active high)
184	UART1_CTSn_SB	UART1_CTSn	I	UART 1 CTS (not available on Z conf.)

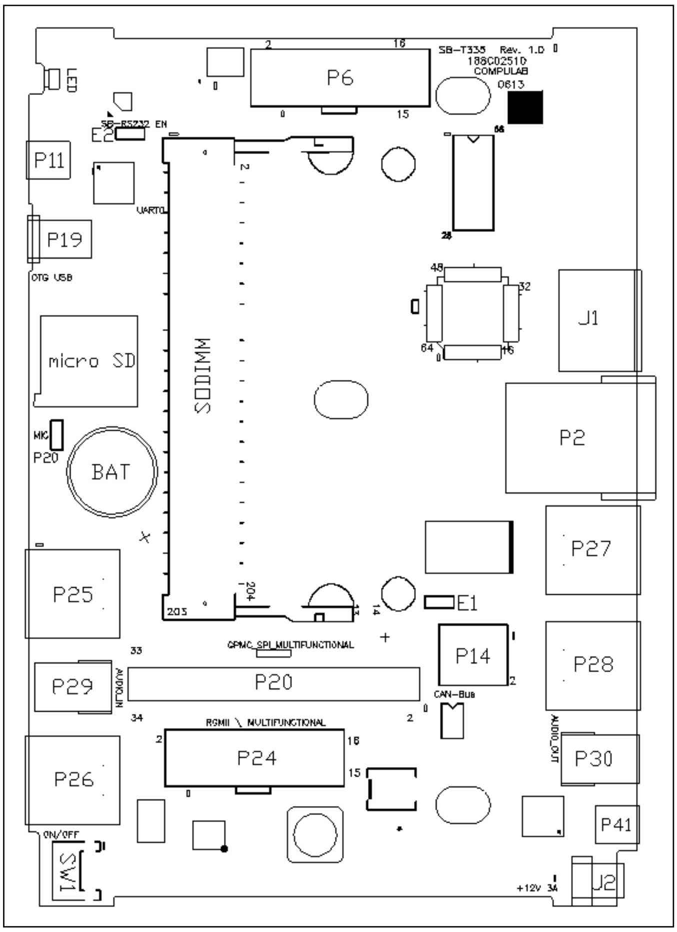
185	USBHUBP1_nOVC		I	USB1 OC sense (PU)
186	UART1_RTSn_SB	UART1_RTSn	O	UART 1 RTS (not available on Z conf.)
187	USB2_CPEN		I	USB2 Power Enable (active high)
188	UART1_TXD_SB	UART1_TXD	O	UART 1 TXD (not available on Z conf.)
189	NC			Not connected
190	USB0_ID		O	USB hub indicator, high active
191	USBHUBP2_nOVC		I	USB2 OC sense (PU)
192	USB0_DN		IO	USB0 Data N
193	GND			Digital ground
194	USB0_DP		IO	USB0 Data P
195	USB3_CPEN		I	USB3 Power Enable (active high)
196	VIN		PWR	Main power supply, 5V typ.
197	USBHUBP3_nOVC		I	USB 3 OC sense (PU)
198	SPI0_DO_SB	SPI0_DO		SPI DO (not available on WB conf.)
199	USB4_CPEN		I	USB4 Power Enable (active high)
200	SPI0_SCLK_SB	SPI0_SCLK		SPI SCLK (not available on WB conf.)
201	USBHUBP4_nOVC		I	USB 4 OC sense (PU)
202	USB0_DRVVBUS	USB0_DRVVBUS	O	USB0 VBUS control (active high)
203	GND			Digital ground
204	GND			Digital ground

For additional information about the CM-T335 interface signals, refer to the CM-T335 SoM Reference Guide.

5 MECHANICAL DRAWINGS

The location of the main components and connectors is depicted in Figure 3.

Figure 3 SB-T335 Mechanical drawing



6 OPERATIONAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

Table 15 Absolute Maximum Ratings

Parameter	Min	Typ.	Max	Unit
Main power supply voltage	-0.3	12	16	V

6.2 Recommended Operating Conditions

Table 16 Recommended Operating Conditions

Parameter	Min	Typ.	Max	Unit
Main power supply voltage	10	12	16	V

6.3 DC Electrical Characteristics

Table 17 DC Electrical Characteristics

Parameter	Operating Conditions	Min	Typ	Max	Unit
3.3V Digital I/O					
V_{IH}		2		3.3	V
V_{IL}		0		0.8	V
V_{OH}		2.85			V
V_{OL}				0.45	V
RS232					
TX Voltage Swing		±5	±5.4		V
RX Voltage Swing			±25		V