SBC-iBT

Reference Guide

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Table 1 Document Revision Notes

Date	Description
December 2014	• First release

1 INTRODUCTION

1.1 About This Document

This document is part of a set of reference documents necessary to operate and program CompuLab SBC-iBT.

1.2 Related Documents

For additional information not covered in this manual, please refer to the documents listed in Table 2.

Table 2 Related Documents

Document	Location
SBC-iBT Resources	http://www.compulab.co.il/products/sbcs/sbc-ibt/

2 OVERVIEW

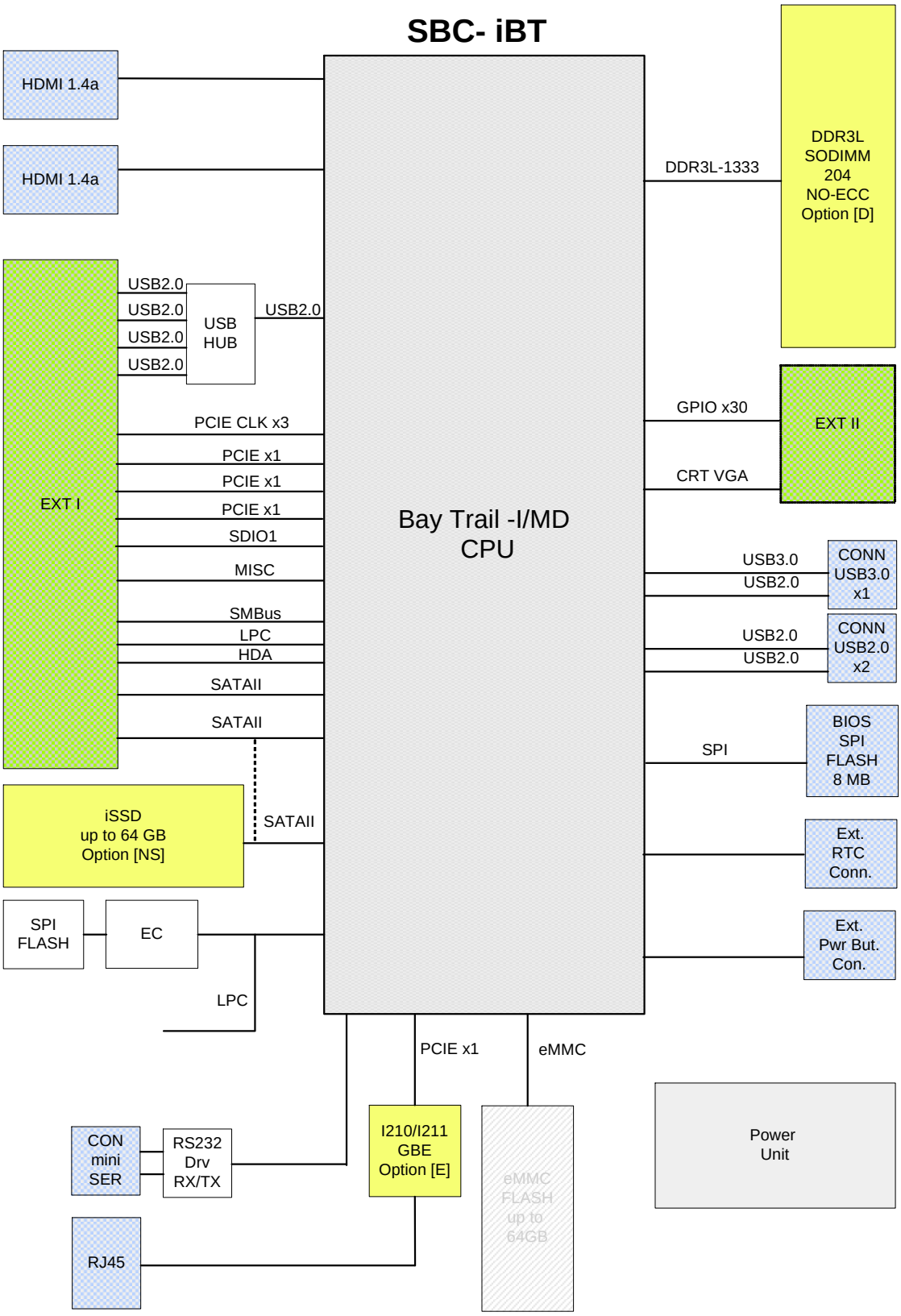
2.1 Highlights

SBC-iBT is an extensible single board computer with powerful multimedia capabilities, based on Intel's Bay Trail SoC.

- Intel's Bay Trail I/M/D Quad core CPU
- Dual head Intel's Generaion7 HD Graphics
- Up to 8GB DDR3L
- Up to 64GB on-board SSD storage
- 2x HDMI 1.4a outputs up to 1980 x 1200 @ 60Hz
- 2xGbE (one using EB-iBT extension)
- USB3, 4 USB2 (2 using EB-iBT extension)
- RS232
- 7.1 Digital audio / 2 CH analog audio /SPDI/F (using EB-iBT extension)
- 2x Mini PCIe (using EB-iBT extension)
- mSATA (using EB-iBT extension)
- 1x micro SIM slot (using EB-iBT extension)
- 7260 Dual band Intel's WiFi + BT4.0 (using EB-iBT extension)
- 3 PCIe x 1, 2 SATA , 4 USB2 , HDA, LPC, SDIO ,VGA ,SMBus , GPIO x30
- Linux, Windows 7 ,Windows Embedded 7, Win8.1 and DOS support
- Miniature size 75 x 116 x 19.6 mm

2.2 Block Diagram

Figure 1 SBC-iBT Block Diagram



2.3 Features

System

Feature	Specifications			Notes
CPU	Bay Trail E3815 64bit Single core 1.46GHz 5W TDP Option [CE3815]	Bay Trail Celeron N2807 64bit Dual core up to 2.16GHz (Burst) 4.3W TDP Option [N2807]	Bay Trail Celeron J1900 64bit Quad core up to 2.41GHz (Burst) 10W TDP Option [CJ1900]	
RAM	Up to 8 GB, DDR3L, 1333 MHz, 64-bit (SO-DIMM sockets)			Option [D]
Storage	On-board SSD up to 64GB			Option [NS]

Graphics

Feature	Specifications			Notes
GPU	Intel HD Graphic	Intel HD Graphic	Intel HD Graphic	
	400 MHz	Up to 750MHz Turbo	Up to 854 MHz Turbo	
HDMI (x2)	Dual port HDMI 1.4a up to 1920x1200 at 60 Hz			

I/O

Feature	Specifications	Notes
Network	1000 BaseT Ethernet port, activity LEDs, RJ-45 connector	Option [E]
USB	USB 3.0 host port, 5 Gbit/s	
	Two USB 2.0 host ports, 480 Mbit/s	
RS232	Partial modem controls, ultra mini serial connector	
	Extension Interfaces • 3x PCIe • 4x USB2 • Up to 2x SATA II • SD memory card • SMBus • 30x GPIOs • LPC • VGA • HDA	

Electrical and Mechanical

Feature	Notes			
Power Supply	Unregulated 9-15V			
Power consumption	Bay Trail E3815	Bay Trail Celeron N2807	Bay Trail Celeron J1900	Depends on system load and assembled options
	2W – 6W	3W – 8W	4W – 12W	
Dimensions	7.5cm x 11.6cm x 1.96cm			

3 CORE SYSTEM COMPONENTS

3.1 Intel Bay Trail SoC

3.1.1 CPU Core

Intel Bay Trail SoC supports the following key features:

- Advanced 22-nm process technology
- Up to four IA-compatible low power Intel x86 processor cores
- One thread per core
- Up to 2MB L2 cache
- INTEL 64 architecture
- Advanced Branch Prediction
- Out-of-Order Instruction Execution
- 64-bit floating-point unit
- SSE4.1,SSE4.2, AES,AES-NI,AVX
- Intel Carry-Less Multiplication Instruction (PCLMULQDQ)
- Digital Random Number Generator (DRNG)
- Intel Virtualization technology (Intel VT-x)

3.1.2 GPU Core

Intel Bay Trail SOC integrated GPU supports the following key features:

- Intel's 7th generation (Gen7) graphics and media encode/decode engine
- VED video decoder in addition to Gen 7 Media decoder
- DirectX 11
- OpenCL 1.2
- OpenGL 3.0
- OpenGLES 2.0
- GPU shader up to 8 gigaflops
- 4x anti-aliasing
- Full HW acceleration for decode H.264,JPEG,MJPEG,MPEG2,VC-1,WMV9
- Full HW acceleration for encode H.264
- Polyphase 8 tap scaling
- HD HQV

3.2 System Memory

3.2.1 DRAM

SBC-iBT features one user accessible DDR3L SO-DIMM socket. The DRAM interface is 64-bits wide and runs up to 666 MHz clock DDR (DDR3L-1333). SBC-iBT supports up to 8GB of memory.

3.3 Display Subsystem

3.3.1 HDMI

SBC-iBT supports two HDMI interfaces –connectors J51 and J54. The HDMI outputs support HDMI 1.4a and resolutions of up to 1920 x 1200 x 24bpp@60Hz.

3.3.2 VGA

SBC-iBT supports internal VGA interface (up to 2500 x 1600@60Hz) routed to the extension connector P30.

3.4 Internal SSD Storage

SBC-iBT features high speed on-board MLC SSD storage with build-in hardware ECC (up to 72bit/1KB) achieving up to 300MB/s sequential read and 160MB/s sequential write with maximum capacity up to 64GB. Internal SSD resides on the SATA0 interface. When not populated SATA0 is routed to the extension connector.

3.5 High Definition Audio (HDA)

The SBC-iBT supports audio streams through HDMI interfaces and provides HDA interface for connection of HDA audio codecs (implemented on the EB-iBT extension)

3.6 USB2.0

The SBC-iBT features four internal USB2.0 interfaces:

- Two interfaces are routed to the external USB2.0 port through dual-stacked U50 connector. The down-stream port support High-speed and Full-speed/Low-speed connections.
- One USB2.0 interface is routed to the USB3.0 connector
- One USB2.0 port connected to the USB2.0 HUB , which outputs 4 additional USB2.0 interfaces to the extension connector P31

3.7 USB3.0

SBC-iBT features one internal USB3.0 interface which supports SuperSpeed, High-speed and Full-speed/Low-speed connections.

The USB down-stream port is routed to the USB3 connector J49.

3.8 Gigabit Ethernet

SBC-iBT Gigabit Ethernet interface is implemented with the I211 Intel Gigabit Ethernet controller. The controller is connected to the PCIe interface. Main features:

- PCIE v2.1 (2.5GT/s) x1
- Jumbo frames
- 802.1q Double VLAN support
- IEEE 1588
- Crossover Detection and Auto-Correction
- Wake-on-LAN and remote wake-up support
- Auto-negotiation
- Activity and speed indicator LED controls

Gigabit Ethernet signals are routed to the RJ-45 connector P26.

3.9 UART

SBC-iBT utilizes internal Bay Trail SoC PCU TX/RX UART routed through the RS232 transceiver to the RS232 connector P4.

3.10 SD

SBC-iBT utilizes internal Bay Trail SoC SD card interface. Main features:

- SD card 3.0 Bus interface
- Up to 400 Mbits per second
- Support for UHS-I modes: HS, DDR50 and SD12/25
- Support for CRC7 for command and CRC16 for data integrity
- IEEE 1588

SBC-iBT supports SD-card boot using DOS Linux and Win8.x OS. The SD drivers for Win7/WES7 are currently not provided by Intel.

4 SYSTEM LOGIC

4.1 Power Subsystem

4.1.1 Power Rails

SBC-iBT is powered with a single 12V power supply through connector J47. SBC-iBT power range is from 9V up to 15V.

4.1.2 RTC

SBC-iBT features external RTC connector P1 for connection of RTC battery pack. Alternatively RTC voltage may be supplied through the pin on an extension connector P1-B34.

Extension board (EB-iBT) features 18mAh rechargeable coin cell lithium battery, which maintains the SBC-iBT RTC when the main power supply is not present. The battery is being re-charged whenever SBC-iBT is connected to the main power supply. The back-up battery will sustain the RTC for up to 4 months with no charging.

SBC-iBT may operate in RTC-less mode (without using of battery), saving all main parameters in the BIOS SPI flash, not including date and time (can be updated through OS network services).

4.1.3 Power-on Logic

SBC-iBT is designed to support standard PC power-on logic. The SBC-iBT BIOS can be configured (using “State after G3” menu) for the following behavior for when main power is applied:

- S5 - Stay off
- S3 - Turn on automatically

4.1.4 Power Button

The SBC-iBT power button SW5 controls the system power state. The button serves as a standard ON/OFF button in a typical PC system. The button behavior is programmable using standard tools available in MS Windows and Linux.

4.1.5 Power LED

SBC-iBT features dual power LED indicators with the following behavior:

- Green- The system is in the ON state
- Red - The system is in the OFF state
- Off – The system is in the Suspend-To-Ram state (sleep ,S3)

5 EXTENSION MODULE INTERFACES

5.1 PCIe

Table 3 PCIe Interface Signals

Signal Name	Pin #	Type	Description	Notes
PCIe-0				
PCIE_TX0+	P31-B44	I/O	PCIe port 0 transmit positive	AC-coupled
PCIE_TX0-	P31-B45	I/O	PCIe port 0 transmit negative	AC-coupled
PCIE_RX0+	P31-A44	I/O	PCIe port 0 receive positive	
PCIE_RX0-	P31-A45	I/O	PCIe port 0 receive negative	
PCIe-1				
PCIE_TX1+	P31-B41	I/O	PCIe port 1 transmit positive	AC-coupled
PCIE_TX1-	P31-B42	I/O	PCIe port 1 transmit negative	AC-coupled
PCIE_RX1+	P31-A41	I/O	PCIe port 1 receive positive	
PCIE_RX1-	P31-A42	I/O	PCIe port 1 receive negative	
PCIe-2				
PCIE_TX2+	P31-B38	I/O	PCIe port 2 transmit positive	AC-coupled
PCIE_TX2-	P31-B39	I/O	PCIe port 2 transmit negative	AC-coupled
PCIE_RX2+	P31-A38	I/O	PCIe port 2 receive positive	
PCIE_RX2-	P31-A39	I/O	PCIe port 2 receive negative	
PCIe generic				
PCIE_CLK0+	P31-B32	O	PCIe clock 0 positive	
PCIE_CLK0-	P31-B33	O	PCIe clock 0 negative	
PCIE_CLK1+	P31-B2	O	PCIe clock 1 positive	
PCIE_CLK1-	P31-B3	O	PCIe clock 1 negative	
PCIE_CLK2+	P31-B5	O	PCIe clock 2 positive	
PCIE_CLK2-	P31-B6	O	PCIe clock 2 negative	
RESET#	P31-B31	O	PCIe reset. Asserted during transition to S3/S4/S5.	
PCIE_WAKE#	P31-A37	I	PCIe wake-up	
CLK_OE#	P31-A22	I	PCIe clock request	

5.2 SATA

Table 4 SATA Interface Signals

Signal Name	Pin #	Type	Description	Notes
SATA-1				
SATA0_TX+(*)	P31-A2	O	SATA channel 1 transmit positive	AC coupled
SATA0_TX-(*)	P31-A3	O	SATA channel 1 transmit negative	AC coupled
SATA0_RX+(*)	P31-A5	I	SATA channel 1 receive positive	AC coupled
SATA0_RX-(*)	P31-A6	I	SATA channel 1 receive negative	AC coupled
SATA-2				
SATA1_TX+	P31-A8	O	SATA channel 2 transmit positive	AC coupled
SATA1_TX-	P31-A9	O	SATA channel 2 transmit negative	AC coupled
SATA1_RX+	P31-A11	I	SATA channel 2 receive positive	AC coupled
SATA1_RX-	P31-A12	I	SATA channel 2 receive negative	AC coupled
SATA generic				
SATA_ACT#	P31-B4	OD	SATA channel active	

*** SATA0* interface is unavailable when internal storage SSD is populated.**

5.3 USB

Table 5 USB Interface Signals

Signal Name	Pin #	Type	Description	Notes
USB-0				
USB0_P	P31-A24	I/O	USB port 0 positive I/O	
USB0_N	P31-A25	I/O	USB port 0 negative I/O	
USB-1				
USB1_P	P31-A27	I/O	USB port 1 positive I/O	
USB1_N	P31-A28	I/O	USB port 1 negative I/O	
USB-2				
USB2_P	P31-B17	I/O	USB port 2 positive I/O	
USB2_N	P31-B18	I/O	USB port 2 negative I/O	
USB-8				
USB3_P	P31-B14	I/O	USB port 3 positive I/O	
USB3_N	P31-B15	I/O	USB port 3 negative I/O	
USB Overcurrent				
USB_OC#	P31-A26	I	USB over current for ports 0 to 3	

5.4 SMBus

Table 6 SMBus Interface Signals

Signal Name	Pin #	Type	Description	Notes
SMBus				
SMB _CLK	P31-A14	I/OD	SMBus clock	
SMB _DAT	P31-A15	I/OD	SMBus data	
SMBus generic				
SMB_ALRT#	P31-A10	I	SMBus alert	

5.5 High Definition Audio (HDA)

Table 7 High Definition Audio (HDA) Interface Signals

Signal Name	Pin #	Type	Description	Notes
HDA_ RST#	P31-A16	O	HD audio interface reset	1.5V tolerant
HDA_SYNC	P31-A17	O	HD audio sync signal to codec	1.5V tolerant
HDA_BITCLK	P31-A18	O	HD audio interface bit clock	1.5V tolerant
HDA_SOUT	P31-A19	O	HD audio serial data output to codec	1.5V tolerant
HDA_SDIN0	P31-A21	I/O	HD audio serial data input from a third codec	1.5V tolerant
Generic				
V1.5S_AUDIO	P31-B21	O	300 mA power output for external HDA codec	

5.6 LPC

Table 8 LPC Interface Signals

Signal Name	Pin #	Type	Description	Notes
LPC_AD0	P31-A30	I/O	Multiplexed command / address / data bit 0	3.3V tolerant
LPC_AD1	P31-A31	I/O	Multiplexed command / address / data bit 1	3.3V tolerant
LPC_AD2	P31-A32	I/O	Multiplexed command / address / data bit 2	3.3V tolerant
LPC_AD3	P31-A33	I/O	Multiplexed command / address / data bit 3	3.3V tolerant
LPC_CLK	P31-B23	O	Clock for LPC devices	3.3V tolerant
LPC_FRAME#	P31-B24	O	LPC bus frame	3.3V tolerant
LPC_SER_IRQ	P31-B22	I/O	Serial IRQ	3.3V tolerant

5.7 SDIO

Table 9 SDIO Interface Signals

Signal Name	Pin #	Type	Description	Notes
SDIO_D0	P31-B27	I/O	SD Card data bit 0	3.3V tolerant
SDIO_D1	P31-B28	I/O	SD Card data bit 1	3.3V tolerant
SDIO_D2	P31-B29	I/O	SD Card data bit 2	3.3V tolerant
SDIO_D3	P31-B30	I/O	SD Card data bit 3	3.3V tolerant
SDIO_CLK	P31-B26	O	SD Card Clock (24 to 50MHz)	3.3V tolerant
SDIO_CMD	P31-B20	O	SD Card Command	3.3V tolerant
SDIO_WP	P30-A30	I	SD Card Write protection, active high	1.8V tolerant 5K PD

Signal Name	Pin #	Type	Description	Notes
Generic				
+VSDIO_EN	P31-B37	O	Provides SD card power control to switch off SDIO power when not in use	

5.8 VGA

Table 10 VGA Interface Signals

Signal Name	Pin #	Type	Description	Notes
CRT_RED	P30-B17	O	Red Analog Video Output	3.3V Tolerant
CRT_GREEN	P30-B18	O	Green Analog Video Output	3.3V Tolerant
CRT_BLUE	P30-B19	O	Blue Analog Video Output	3.3V Tolerant
CRT_VSYNC	P30-B21	O	VGA Horizontal Synchronization	3.3V Tolerant
CRT_HSYNC	P30-B22	O	VGA Horizontal Synchronization	3.3V Tolerant
CRT_DDC_CLK	P30-B35	I/O	EDID support for an external display	3.3V Tolerant
CRT_DDC_DATA	P30-B36	I/O	EDID support for an external display	3.3V Tolerant

5.9 GPIOs

Table 11 GPIO/MUXED Signals

Signal Name	Pin #	Type	Description	Notes
GPIO_S0_SC[078]	P30-A2	I/O	S0-domain General Purpose I/O All GPIOs are 1.8V tolerant	20K PU 1.8V
GPIO_S0_SC[079]	P30-A3			20K PU 1.8V
GPIO_S0_SC[080]	P30-A4			20K PU 1.8V
GPIO_S0_SC[081]	P30-A5			20K PU 1.8V
GPIO_S0_SC[082]	P30-A6			20K PU 1.8V
GPIO_S0_SC[083]	P30-A7			20K PU 1.8V
GPIO_S0_SC[084]	P30-A8			20K PU 1.8V
GPIO_S0_SC[085]	P30-A9			20K PU 1.8V
GPIO_S0_SC[086]	P30-A10			20K PU 1.8V
GPIO_S0_SC[087]	P30-A11			20K PU 1.8V
GPIO_S0_SC[088]	P30-A12			20K PU 1.8V
GPIO_S0_SC[089]	P30-A14			20K PU 1.8V
GPIO_S0_SC[090]	P30-A15			20K PU 1.8V
GPIO_S0_SC[091]	P30-A16			20K PU 1.8V
GPIO_S0_SC[092]	P30-A17			20K PU 1.8V
GPIO_S0_SC[093]	P30-A18			20K PU 1.8V
GPIO_S0_SC[032]	P30-A23			20K PU 1.8V
GPIO_S0_SC[027]	P30-A24			20K PD
GPIO_S0_SC[028]	P30-A26			20K PU 1.8V
GPIO_S0_SC[029]	P30-A27			20K PU 1.8V
GPIO_S0_SC[030]	P30-A28			20K PU 1.8V
GPIO_S0_SC[037]	P30-A29			20K PU 1.8V
GPIO_S0_SC[071]	P30-B30			20K PU 1.8V
GPIO_S0_SC[070]	P30-B31			20K PU 1.8V
GPIO_S0_SC[072]	P30-B32			20K PU 1.8V
GPIO_S0_SC[073]	P30-B33			20K PU 1.8V
GPIO_S0_SC[075]	P30-B38			20K PU 1.8V
GPIO_S0_SC[074]	P30-B39			20K PU 1.8V
GPIO_S0_SC[076]	P30-B41			20K PU 1.8V
GPIO_S0_SC[077]	P30-B42			20K PU 1.8V

NOTE: GPIO numbering corresponds with GPIO numbering in the E3800 SoC documentation. Since all GPIOs are 1.8V tolerant level shifter should be used in case of using 3.3V domains

5.10 Power

Table 12 Power Signals

Signal Name	Pin #	Type	Description	Available
GND	P31-A1, P31-B1, P31-A7, P31-A23, P31-B25, P31-A29, P31-A34, P31-A40, P31-B40, P30-A1, P30-B1, P30-B7, P30-B10, P30-B16, P30-B23, P30-A25, P30-B26, P30-B29, P30-A31, P30-B34, P30-A40, P30-B40	P	Main GND rail 22 pins	
V1.2S	P30-B37	P	S0-domain 1.2V power rail Providing up to 500mA (max) 1 pin	S0
V1.8S	P30-A20, P30-A21, P30-A22, P30-B20	P	S0-domain 1.8V power rail Providing up to 1A (max) 4 pins	S0
V3.3S	P31-B9, P31-B11, P31-B12, P30-B35, P31-B4, P31-A13, P31-B13	P	S0-domain 3.3V power rail Providing up to 3A (max) 7 pins	S0
V3.3SBY	P31-A36, P31-A46, P31-B46, P31-B16, P30-A46, P30-A47, P30-A48, P30-B46, P30-B47	P	S5-domain 3.3V power rail Providing up to 4A (max) 9 pins	S0,S3,S5
V5SBY	P31-A4, P31-B7, P31-B8, P31-A13, P31-B13, P31-B19	P	S5-domain 5V power rail Providing up to 6A (max) 6 pins	S0,S3,S5
VCC_12V	P31-A47, P31-A48, P31-A49, P31-A50, P31-B47, P31-B48, P31-B49, P31-B50	P	S5-domain main 12V power rail. May be used as input to the SBC-iBT if input power supplied through extension board 8 pins	S0,S3,S5

5.11 Miscellaneous

Table 13 Miscellaneous Signals

Signal Name	Pin #	Type	Description	Notes
PWRBTN#	P31-A43	I	Power button - causes an SMI or SCI to indicate a system request to enter a sleep state. If the system is already in a sleep state, this signal will cause a wake event. If PWR_BTN# is asserted for more than 4 seconds, it will cause an unconditional transition (power button override) to the S5 state with only the PWR_BTN# available as a wake event. Override will occur even if the system is in the S1 state. This signal has an internal pull-up resistor.	10K PU to V3.3SBY
SLP_S3#	P31-B43	OD	S3 sleep power plane control. Assertion of SLP_S3# shuts off power to non-critical components when system transitions to S3 or S5 states. De-assertion of SLP_S3# turns on power to non-critical components when system transitions from S3 or S5 back to S0.	10K PU to V3.3SBY
SLP_S4#	P31-B10	OD	S4 sleep power plane control. Assertion of SLP_S4# shuts all powers off excluding S5 domain.	10K PU to V3.3SBY
CLK_25MHZ	P31-A35	O	25MHz clock for the external devices	
mSATA_GPIO	P31-A20	O	GPIO used to control of external mux for switching between mSATA and PCIE	2k PU to 1.8A 1.8V tolerant
RESERVED	P30-A19, P30-A32, P30-A33, P30-A34, P30-A35, P30-A36, P30-A37, P30-A38, P30-A39, P30-A41, P30-A42, P40-A43, P30-A44, P30-A45, P30-B49, P30-A50, P30-B2, P30-B3, P30-B5, P30-B6, P30-B8,P30-B9, P30-11, P30-B12,P30-B14, P30-B15, P30-B24, P30-B25, P30-B27, P30-B28, P30-B43, P30-B45, P30-B48, P30-B49, P30-B50	-	Reserved for internal/future use. Should be left unconnected. 34 pins	
NC	P31-B36, P30-B44		Not connected pins Should be left unconnected 2 pins	

6 CONNECTORS

6.1 HDMI1 Connector (J51)

The HDMI display output is provided through the standard HDMI socket (J51).

For additional details, please refer to section 3.3.1 of this document.

6.2 HDMI2 Connector (J54)

The HDMI display output is provided through the standard HDMI socket (J54).

For additional details, please refer to section 3.3.1 of this document.

6.3 DC Power Jack (J47)

DC power input connector.

Table 14 J47 connector pin-out

Pin	Signal Name
1	+V12
2	GND

Table 15 J47 connector data

Manufacturer	Mfg. P/N
Contact Technology	DC-081HS

The connector is compatible with the SBC-iBT power supply unit supplied by CompuLab.

SBC-iBT has internal reverse polarity protection circuit when power is supplied through J47 connector.

6.4 RS232 connector (P4)

The SBC-iBT RS232 port is routed to the on-board RS232 ultra-mini connector (P2). All signals are at RS232 levels.

Table 16 P4 connector pin-out

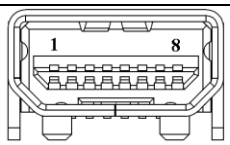
Pin	Signal Name	Pin	Signal Name	
1	RS232_TXD	5	RS232_DTR	
3	RS232_RXD	7	RS232_RI	

Table 17 P4 connector data

Manufacturer	Mfg. P/N	Mating connector
Wieson	G3169-500001	Wieson, P/N: 4306-5000

The connector is compatible with the serial cable adapter (CompuLab P/N 199D10230) supplied by CompuLab.

6.5 USB 3.0 Host Connectors (J49)

The SBC-iBT USB3.0 host ports are available through a single USB 3.0 standard type-A connector (J49).

6.6 USB 2.0 Host Connectors (U50)

The SBC-iBT USB2.0 host ports are available through a dual-stacked USB 2.0 standard type-A connector (U50).

6.7 Gigabit Ethernet Connector (P26)

The SBC-iBT Gigabit Ethernet port is routed to the standard RJ-45 connector (P26).

6.8 SO-DIMM Socket (J43)

The SBC-iBT features two standard DDR3L 204-pin SO-DIMM socket – J43.

6.9 External RTC connector (P1)

The SBC-iBT features connector for the external RTC battery.

Table 186 P1 connector pin-out

Pin	Signal Name
1	GND
2	+VCCRTC (2.6-3.1V)

Table 17 P1 connector data

Manufacturer	Mfg. P/N	Mating parts
Molex	53261-0271	Terminals: Molex P/N 50058-8000 Housing Molex P/N 51021-0200 Wires UL1571 AWG#30

Compulab provides assembled pack:

Table 18 External battery pack

Manufacturer	Mfg. P/N	Description
Compulab	507A010010M	Assembled Battery, BR1632A, High Temp, 3V/120mA, 2 wire, W2B connector

6.10 External power button (P2)

SBC-iBT features connector for the external RTC battery.

Table 19 P2 connector pin-out

Pin	Signal Name
1	GND
2	PWRBTN#

Table 20 P2 connector data

Manufacturer	Mfg. P/N	Mating parts
Molex	53261-0271	Terminals: Molex P/N 50058-8000 Housing Molex P/N 51021-0200 Wires UL1571 AWG#30

6.11 Extension Connectors (P31, P30)

Table 20 P31 connector pin-out

Pin	Signal Name	Pin	Signal Name
A1	GND	B1	GND
A2	SATA0_TX+	B2	PCIE_CLK1+
A3	SATA0_TX-	B3	PCIE_CLK1-
A4	V5SBY	B4	SATA0_LED
A5	SATA0_RX+	B5	PCIE_CLK2+
A6	SATA0_RX-	B6	PCIE_CLK2-
A7	GND	B7	V5SBY
A8	SATA1_TX+	B8	V5SBY
A9	SATA1_TX-	B9	V3.3S
A10	SMB_ALRT#	B10	SLP_S4#
A11	SATA1_RX+	B11	V3.3S
A12	SATA1_RX-	B12	V3.3S
A13	V5SBY	B13	V5SBY
A14	SMB_CLK	B14	USB3_P
A15	SMB_DAT	B15	USB3_N
A16	HDA_RST#	B16	V3.3SBY
A17	HDA_SYNC	B17	USB2_P
A18	HDA_BITCLK	B18	USB2_N
A19	HDA_SDOUT	B19	V5SBY
A20	GPIO	B20	SDIO_CMD
A21	HDA_SDIN0	B21	V1.5S_AUDIO
A22	CLK_OE#	B22	LPC_SERIRQ
A23	GND	B23	LPC_CLK
A24	USB0_P	B24	LPC_FRAME#
A25	USB0_N	B25	GND
A26	USB_OC#	B26	SDIO_CLK
A27	USB1_P	B27	SDIO_D0
A28	USB1_N	B28	SDIO_D1
A29	GND	B29	SDIO_D2
A30	LPC_AD0	B30	SDIO_D3
A31	LPC_AD1	B31	RESET#
A32	LPC_AD2	B32	PCIE_CLK0+
A33	LPC_AD3	B33	PCIE_CLK0-
A34	GND	B34	VCCRTC
A35	CLK_25MHZ	B35	V3.3S
A36	V3.3SBY	B36	RESERVED
A37	PCIE_WAKE#	B37	SDIO_PWR_EN#
A38	PCIE_RX2+	B38	PCIE_TX2+
A39	PCIE_RX2-	B39	PCIE_TX2-
A40	GND	B40	GND
A41	PCIE_RX1+	B41	PCIE_TX1+
A42	PCIE_RX1-	B42	PCIE_TX1-
A43	PWRBTN#	B43	SLP_S3#
A44	PCIE_RX0+	B44	PCIE_TX0+
A45	PCIE_RX0-	B45	PCIE_TX0-
A46	V3.3SBY	B46	V3.3SBY
A47	VCC_12V	B47	VCC_12V
A48	VCC_12V	B48	VCC_12V
A49	VCC_12V	B49	VCC_12V
A50	VCC_12V	B50	VCC_12V

Table 21 P30 connector pin-out

Pin	Signal Name	Pin	Signal Name
A1	GND	B1	GND
A2	GPIO_S0_SC[078]	B2	RESERVED
A3	GPIO_S0_SC[079]	B3	RESERVED
A4	GPIO_S0_SC[080]	B4	V3.3S
A5	GPIO_S0_SC[081]	B5	RESERVED
A6	GPIO_S0_SC[082]	B6	RESERVED
A7	GPIO_S0_SC[083]	B7	GND
A8	GPIO_S0_SC[084]	B8	RESERVED
A9	GPIO_S0_SC[085]	B9	RESERVED
A10	GPIO_S0_SC[086]	B10	GND
A11	GPIO_S0_SC[087]	B11	RESERVED
A12	GPIO_S0_SC[088]	B12	RESERVED
A13	V3.3S	B13	V3.3S
A14	GPIO_S0_SC[089]	B14	RESERVED
A15	GPIO_S0_SC[090]	B15	RESERVED
A16	GPIO_S0_SC[091]	B16	GND
A17	GPIO_S0_SC[092]	B17	CRT_RED
A18	GPIO_S0_SC[093]	B18	CRT_BLUE
A19	RESERVED	B19	CRT_GREEN
A20	V1.8S	B20	V1.8S
A21	V1.8S	B21	CRT_VSYNC
A22	V1.8S	B22	CRT_HSYNC
A23	GPIO_S0_SC[032]	B23	GND
A24	GPIO_S0_SC[027]	B24	RESERVED
A25	GND	B25	RESERVED
A26	GPIO_S0_SC[028]	B26	GND
A27	GPIO_S0_SC[029]	B27	RESERVED
A28	GPIO_S0_SC[030]	B28	RESERVED
A29	GPIO_S0_SC[037]	B29	GND
A30	SDIO_WP	B30	GPIO_S0_SC[071]
A31	GND	B31	GPIO_S0_SC[070]
A32	RESERVED	B32	GPIO_S0_SC[072]
A33	RESERVED	B33	GPIO_S0_SC[073]
A34	RESERVED	B34	GND
A35	RESERVED	B35	CRT_DDC_CLK
A36	RESERVED	B36	CRT_DDC_DAT
A37	RESERVED	B37	V1.2S
A38	RESERVED	B38	GPIO_S0_SC[075]
A39	RESERVED	B39	GPIO_S0_SC[074]
A40	GND	B40	GND
A41	RESERVED	B41	GPIO_S0_SC[076]
A42	RESERVED	B42	GPIO_S0_SC[077]
A43	RESERVED	B43	RESERVED
A44	RESERVED	B44	RESERVED
A45	RESERVED	B45	RESERVED
A46	V3.3SBY	B46	V3.3SBY
A47	V3.3SBY	B47	V3.3SBY
A48	V3.3SBY	B48	RESERVED
A49	RESERVED	B49	RESERVED
A50	RESERVED	B50	RESERVED

Table 22 P31, P30 connector data

Manufacturer	Mfg. P/N	Mating connector
FCI	61082-10260[2|6]LF	61083-10460[2|6]LF

6.12 Power Button (SW5)

The SBC-iBT power button SW5 controls the system power state. For additional details, please refer to section 4.1.3 of this document.

7 MECHANICAL DRAWINGS

The mechanical drawings below are provided for connector location information.

Full mechanical drawings are available at www.compulab.co.il/products/sbcs/sbc-ibt/#devres

Figure 2 SBC-iBT top

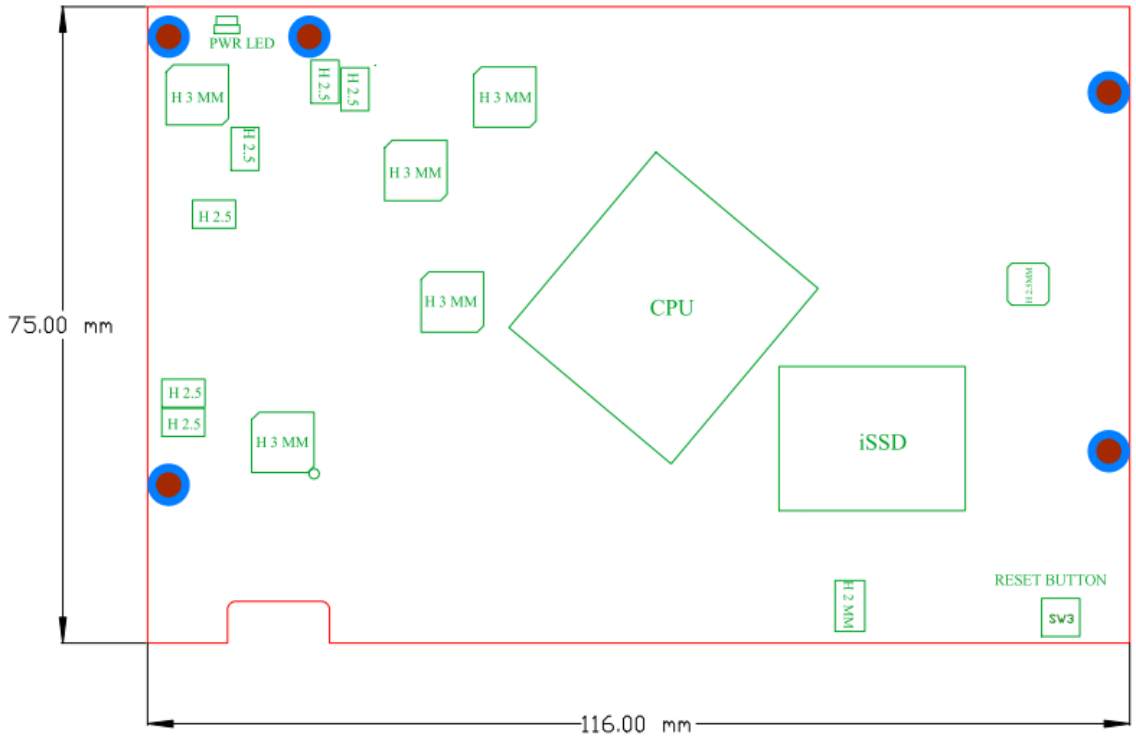
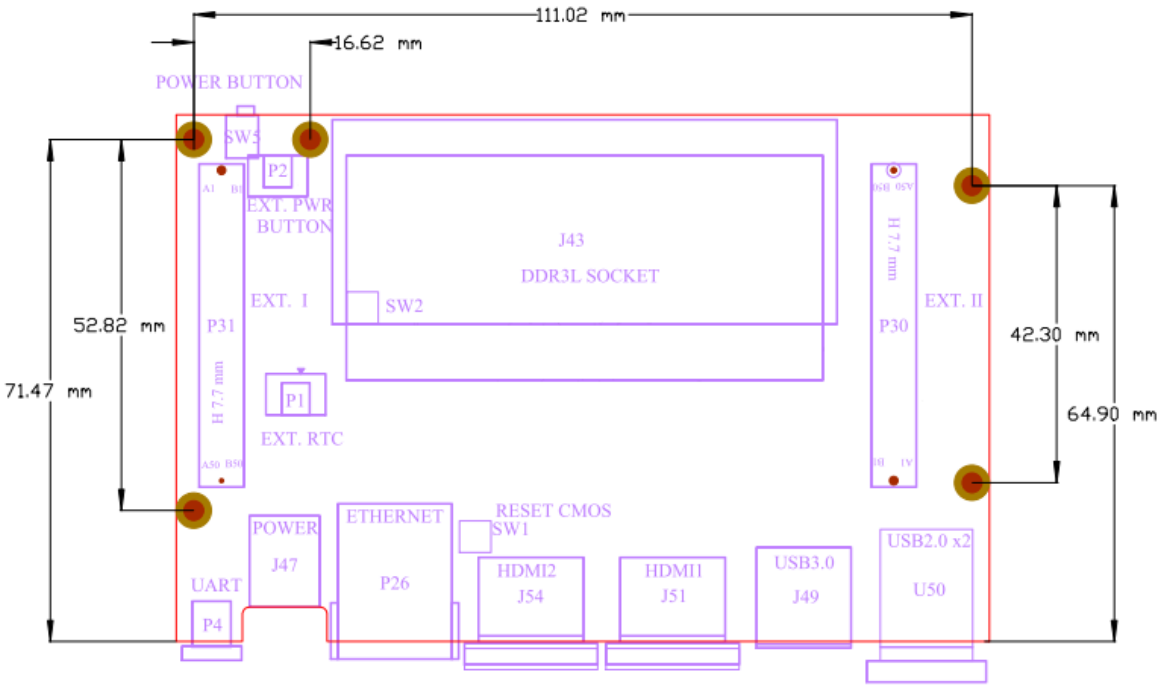


Figure 3 SBC-iBT mother-board bottom (x-ray view - as seen from top side)



8 OPERATIONAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

Table 23 Absolute Maximum Ratings

Parameter	Min	Typ.	Max	Unit
Main power supply voltage	-0.3	12	16	V

NOTE: Stresses beyond Absolute Maximum Ratings may cause permanent damage to the device.

8.2 Recommended Operating Conditions

Table 24 Recommended Operating Conditions

Parameter	Min	Typ.	Max	Unit
Main power supply voltage	9	12	15	V