CM-QS600 CoM

Reference Guide

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Table 1 Revision Notes

Date	Description
June 2014	First release
August 2015	Corrected pin assignment in table 36 and paragraphs: 4.2.1, 4.2.3, 4.3, 4.8.1, 4.12

Please check for a newer revision of this manual at the CompuLab web site http://www.compulab.co.il/. Compare the revision notes of the updated manual from the web site with those of the printed or electronic version you have.

1 INTRODUCTION

1.1 About This Document

This document is part of a set of reference documents providing information necessary to operate and program CompuLab CM-QS600 Computer-on-Module.

1.2 CM-QS600 Part Number Legend

Please refer to the CompuLab website 'Ordering information' section to decode the CM-QS600 part number: https://compulab.co.il/products/computer-on-modules/cm-qs600/#ordering.

1.3 Related Documents

For additional information, refer to the documents listed in Table 2.

Table 2 Related Documents

Document	Location
CM-QS600 Developer Resources	http://www.compulab.co.il

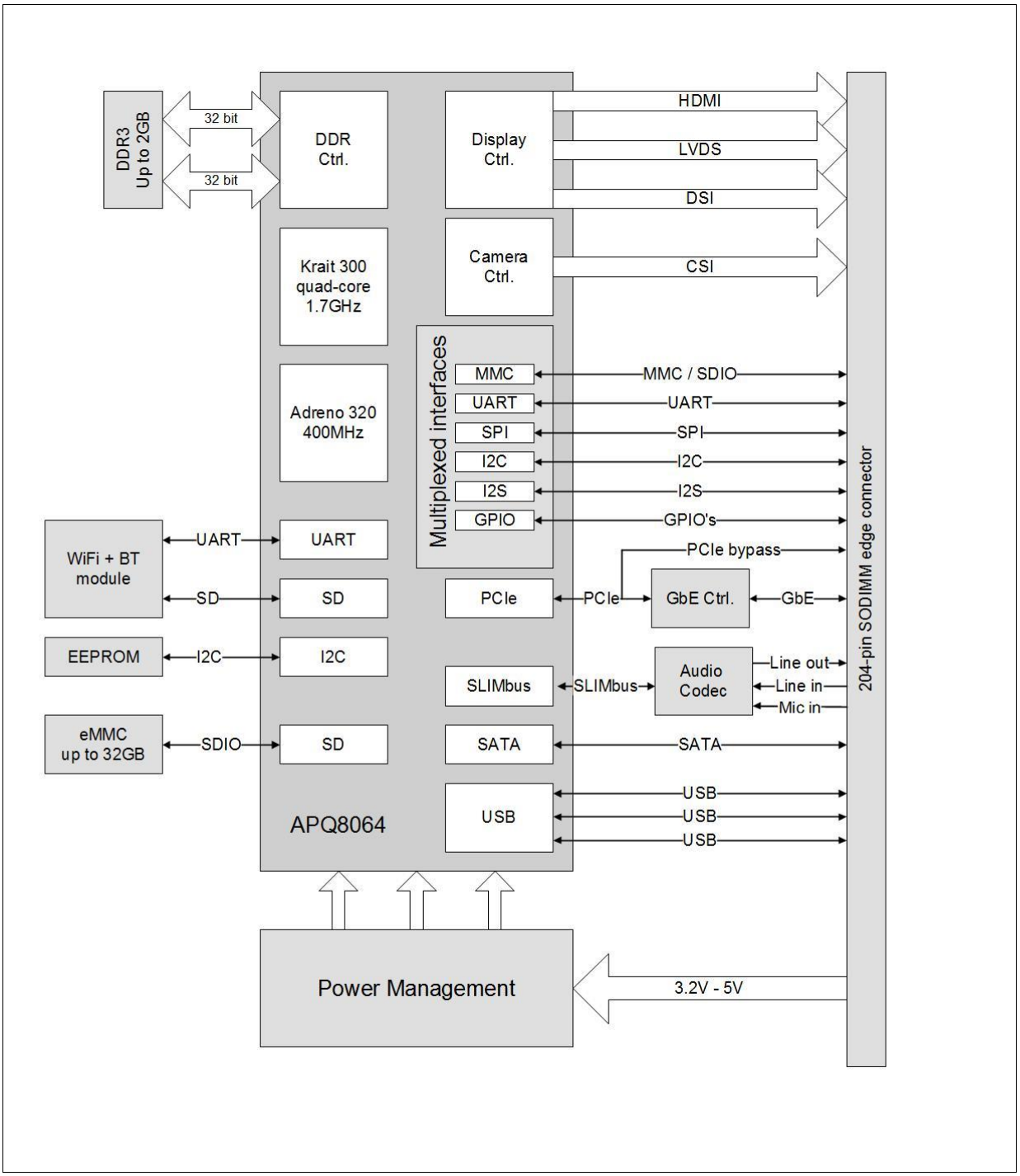
2 OVERVIEW

2.1 Highlights

- Qualcomm Snapdragon APQ8064 quad-core Krait 300 CPU, up to 1.7GHz NEON SIMD and VFPv4
- Up to 2GB Dual Channel DDR3
- Up to 32GB on-board eMMC storage
- Adreno 320 GPU compliant with OpenGL ES 1.1 / 2.0 / 3.0 and OpenCL
- Hexagon QDSP6 for ultra-low power applications
- Multimedia video sub-system supports HD decoding / encoding up-to 1080, H.264, MPEG2/4, DivX and VC-1
- IVA-HD hardware accelerators enable full HD, multi-standard video encode/decode as well as stereoscopic 3D (S3D)
- HDMI 1.4a, LVDS, SATA I (1.5Gbps), USB2.0 OTG x 1, USB2.0 Host x2, UART x5, SPI x5, I2C x5 SDIO x3, Onboard WiFi 802.11b/g/n (2.4GHz), Bluetooth 4.0.
- Miniature size: 65 x 68 x 5 mm
- SB-QS600 carrier board turns the CM-QS600 module into SBC-QS600 - a single board computer

2.2 Block Diagram

Figure 1 CM-QS600 Block Diagram



2.3 CM-QS600 Features

The "Option" column specifies the configuration code required to have the particular feature. "+" means that the feature is always available. Strikethrough option means that the option must not be chosen for the feature to be available.

Table 3 System and Graphics

Feature	Specifications	Option
CPU	Qualcomm Snapdragon 600 APQ8064 quad-core Krait 300, 1.7GHz NEON SIMD and VFPv4 Hexagon QDSP6 for ultra-low power applications	C1700
RAM	512MB - 2GB, Dual Channel DDR3-1066 with 32-bit bus width.	D
Storage	On-board eMMC flash, 4GB to 32GB	N
Video Processing Unit	Multimedia video sub-system supports HD decoding / encoding Up-to 1080, H.264, MPEG2/4, DivX and VC-1	+
Graphics Acceleration Units	Adreno 320 GPU compliant with OpenGL ES 1.1 / 2.0 / 3.0 and OpenCL	+

Table 4 I/O

Feature	Specifications	Option
Display	1x HDMI display interface (with HDMI Audio support)	+
	1x LVDS Display interface	+
USB2.0 Host	2x USB2.0 high-speed host ports, 480Mbps	+
USB2.0 OTG	1x USB2.0 high-speed OTG port, 480Mbps	+
SATA	1x SATA I interface, 1.5 Gbps, integrated controller and PHY	+
Ethernet	1000Base-T Ethernet interface implemented with the Atheros AR8151-B controller	E
Serial Ports (UARTs)	1x UART debug port - TX, RX Only, 1.8V levels (GSBI7)	+
	4x UART ports - TX, RX, CTS, RTS Only, 1.8V levels (GSBI2, GSBI3, GSBI4, GSBI5)	+
	1x UART ports - TX, RX, CTS, RTS Only, 1.8V levels (GSBI6).	NOT WB
I2C	4x I2C interfaces (GSBI2, GSBI3, GSBI4, GSBI5)	+
	1x I2C interfaces (GSBI6)	NOT WB
SPI	4x SPI interfaces (GSBI2, GSBI3, GSBI4, GSBI5).	
	1x SPI interfaces (GSBI6)	NOT WB
Audio	1x On-board audio codec with analog stereo output, stereo input and electret microphone support	A
	1x I2S compliant output interface, 1x I2S input interface	+
	HDMI audio output	+
Camera	1x Quad Lane MIPI-CSI compatible serial camera interface	+
RTC	Real time clock, powered by external lithium battery	+
MMC/SD/SDIO	2x MMC/SD/SDIO ports 1/4-bit transfer modes. (SDCARD – bootable, SDIO3)	+
	1x MMC/SD/SDIO port 1/4-bit transfer modes. (WLSDIO)	NOT WB
WiFi and Bluetooth	Implements 802.11b/g/n wireless connectivity standard Implemented with Atheros QCA6234. Two on-board connectors for external antennas Bluetooth 4.0 (low energy) (also compliant with Bluetooth 2.1 + EDR)	WB
General Purpose I/O	Up to 77 multifunctional signals. Can be used as GPIOs (shared with other functions)	+

Table 5 Electrical, Mechanical and Environmental Specifications

Supply Voltage	4.5V to 5.5V or 3.3V to 4.2 via battery interface
Active power consumption	TBD
Standby/Sleep consumption	TBD
Dimensions	65 x 68 x 5 mm
Weight	30 gram
MTBF	> 100,000 hours
Operation temperature (case)	Commercial: 0º to 70º C Extended: -20º to 70º C Industrial: -40º to 85º C

Storage temperature	-40º to 85º C
Relative humidity	10% to 90% (operation) 05% to 95% (storage)
Shock	50G / 20 ms
Vibration	20G / 0 - 600 Hz
Connectors	SODIMM-204

3 CORE SYSTEM COMPONENTS

3.1 APQ8064 SoC

The Qualcomm APQ8064 SoC is a multimedia application device featuring Snapdragon S600 processor, video, image and graphics processing for a broad range of multimedia-rich applications. The device is composed of the following major subsystems:

- Four Krait application processors – advanced CPU architecture for high-end multimedia applications
  - Up to 1.7 GHz core speed
  - 2 MB L2 cache (combined)
  - ARM v7 compliant
  - TrustZone support
  - VeNum 128-bit SIMD multimedia coprocessor and VFPv4
- Adreno 320 GPU
- Video playback and capture sub-system
- QDSP6 core (500 MHz) for application support
- ARM9 for WLAN/BT/FM processing
- ARM7 for smart peripheral sub-system processing

3.1.1 Video

- 1080p encode and decode at up to 60 fps
- H.263, H.264, MP4

3.1.2 Graphics

APQ8064 incorporates powerful Adreno 320 GPU, optimized specifically for a mobile applications screen size and color depth using low-power, high-performance processing.

- 200 M peak triangles/second
- 6.4 B vector shader instructions/second
- 3.2 BP/second; 3.2 B texel/second
- APIs include OpenGL ES 1.x, 2.0, and 3.0; Direct3D Dx9.x; C2D for 2D composition; OpenCL for Adreno 320
- Direct 3D mobile, flash10-pixel blender acceleration
- 325 MHz and 400 MHz turbo mode

3.1.3 Web technologies – V8 JavaScript Engine optimizations

- Webkit browser JPEG hardware decode acceleration
- Webkit compositing engine 2D/VG GPU acceleration
- Networking Stack IP and HTTP tuning
- Flash 10.1 3D/GL-ES GPU acceleration
- Flash 10.1 and Video Processor/QDSP Video (H.264, VP6, Spark) decode optimization

3.2 Memory

3.2.1 DRAM

CM-QS600 is equipped with up to 2GB of onboard dual-channel DDR3 memory. Each DDR3 channel is 32-bits wide and operates at 533 MHz clock frequency (DDR3-1066).

3.2.2 On-board eMMC storage

CM-QS600 is available with onboard eMMC storage. An eMMC is the main non-volatile memory of CM-QS600. It is used for boot-loader, operating system and general purpose data storage. CM-QS600 (depending on board configuration) can be equipped with a 4GB, 8GB, or 32GB eMMC device.

4 PERIPHERAL INTERFACES

CM-QS600 implements a variety of peripheral interfaces through the SODIMM-204 carrier board connector. The following notes apply to interfaces available through the SODIMM-204 interface:

- Some interfaces/signals are available only with/without certain configuration options of the CM-QS600 CoM. The availability restrictions of each signal are described in the "Signals description" table for each interface.
- Some of the CM-QS600 carrier board interface pins are multifunctional. Up-to 3 functions (ALT modes) are accessible through each multifunctional pin. Multifunctional pins are denoted with an asterisk (*). For additional details, please refer to chapter 5.6.
- All of the CM-QS600 digital interfaces operate at 1.8V voltage levels, unless otherwise noted.

The signals for each interface are described in the "Signal description" table for the interface in question. The following notes provide information on the "Signal description" tables:

- **"Signal name"** – The name of each signal with regards to the discussed interface. The signal name corresponds to the relevant function in cases where the carrier board pin in question is multifunctional.
- **"Pin#" –** The carrier board interface pin number where the discussed signal is available, multifunctional pins are denoted with an asterisk.
- **"Type" –** Signal type, see the definition of different signal types below
- **"Description" –** Signal description with regards to the interface in question.
- **"Availability" –** Depending on CM-QS600 Configuration options, certain carrier board interface pins are physically disconnected (floating) on-board CM-QS600. The "Availability" column summarizes configuration requirements for each signal. All the listed requirements must be met (logical AND) for a signal to be "available" unless otherwise noted.

Each described signal can be one of the following types. Signal type is noted in the "Signal description" tables. Multifunctional pin direction, pull resistor and open drain functionality is software controlled. The "Type" column header for multifunctional pins refers to the recommended pin configuration with regards to the discussed signal.

- **"AI"** – Analog Input
- **"AO"** – Analog Output
- **"AIO"** – Analog Input/Output
- **"AP"** – Analog Power Output
- **"I"** – Digital Input
- **"O"** – Digital Output
- **"IO"** – Digital Input/Output
- **"OD"** – Open Drain Signal (not pulled up on-board CM-QS600 unless otherwise noted).
- **"P"** – Power
- **"PD" -** Always pulled down on-board CM-QS600, (typ. 5KΩ-15KΩ).

4.1 Serial ATA Interface

CM-QS600 incorporates a single SATA port implemented with the APQ8064 integrated SATA controller and PHY. The interface supports the following main features:

- SATA 1.5 Gb/s

Table 6 SATA signals

Signal Name	Pin #	Type	Description	Availability
CPU_SATA_RX_N	29	AI	SATA receive data pair	Always available
CPU_SATA_RX_P	27	AI		Always available
CPU_SATA_TX_N	23	AO	SATA transmit data pair	Always available
CPU_SATA_TX_P	21	AO		Always available

4.2 Display Interfaces

CM-QS600 display subsystem is responsible for grabbing an image from the system memory (frame buffer) and displaying that image on an LCD panel or a TV set. CM-QS600 supports two display interfaces:

- HDMI 1.4a – up-to 1920x1080
- LVDS – Dual channel, up-to 2048x1536
- DSI - 4-lane MIPI_DSI, up to 2048 × 1536

4.2.1 High-Definition Multimedia Interface (HDMI)

The HDMI interface available with CM-QS600 is based on the HDMI module of the APQ8064 SoC. The video data sourced into the HDMI module from the MDP module. The HDMI module supports the following standards & features:

- HDMI Tx core and HDMI PHY 1080p at 60 Hz refresh
- 24-bit RGB color
- Up to 8-channel audio for 7.1 surround sound
- Dolby Digital Plus
- Dolby True-HD
- DTS-HD Master

Table 7 HDMI signals

Signal Name	Pin #	Type	Description	Availability
CLK_165M_HDMI_P	30	AO	TMDS clock pair	Always available
CLK_165M_HDMI_N	32	AO		Always available
HDMI_TX0_P	36	AO	TMDS data 0 pair	Always available
HDMI_TX0_N	38	AO		Always available
HDMI_TX1_P	42	AO	TMDS data 1 pair	Always available
HDMI_TX1_N	44	AO		Always available
HDMI_TX2_P	48	AO	TMDS data 2 pair	Always available
HDMI_TX2_N	50	AO		Always available
HDMI_CEC	34*	IO	Consumer Electronics Control signal	Always available
HDMI_HPD	40*	I	Hot Plug Detect signal	Always available
HDMI_DDC_SCL	25*	O	VESA Data Display Channel clock signal	Always available
HDMI_DDC_SDA	31*	IO	VESA Data Display Channel data signal	Always available

4.2.2 LVDS Display interface

The LVDS interface can be used as a primary display interface with a resolution of up to QXGA

Table 8 LVDS Display Interfaces signals

Signal Name	Pin #	Type	Description	Availability
CLK_170M_0_LVDS_N	35	AO	Differential clock 0 pair	Always available
CLK_170M_0_LVDS_P	33	AO		
LVDS_TX0_N	41	AO	Differential data 0 pair	Always available
LVDS_TX0_P	39	AO		
LVDS_TX1_N	47	AO	Differential data 1 pair	Always available
LVDS_TX1_P	45	AO		
LVDS_TX2_N	53	AO	Differential data 2 pair	Always available
LVDS_TX2_P	51	AO		
LVDS_TX3_N	59	AO	Differential data 3 pair	Always available
LVDS_TX3_P	57	AO		
CLK_170M_1_LVDS_N	76	AO	Differential clock 1 pair	Always available
CLK_170M_1_LVDS_P	74	AO		
LVDS_TX4_N	77	AO	Differential data 4 pair	Always available
LVDS_TX4_P	75	AO		
LVDS_TX5_N	81	AO	Differential data 5 pair	Always available
LVDS_TX5_P	79	AO		
LVDS_TX6_N	99	AO	Differential data 6 pair	Always available
LVDS_TX6_P	97	AO		
LVDS_TX7_N	103	AO	Differential data 7 pair	Always available
LVDS_TX7_P	101	AO		

4.2.3 Display Serial Interface

The LVDS interface can be used as a primary display interface with a resolution of up to QXGA

Table 9 DSI Display Interfaces signals

Signal Name	Pin #	Type	Description	Availability
MIPI_DSI0_CLK_P	173	AO	Differential clock 0 pair	Always available
MIPI_DSI0_CLK_N	175	AO		
MIPI_DSI0_LN0_P	194	AO	Differential data 0 pair	Always available
MIPI_DSI0_LN0_N	196	AO		
MIPI_DSI0_LN1_P	188	AO	Differential data 1 pair	Always available
MIPI_DSI0_LN1_N	190	AO		
MIPI_DSI0_LN2_P	182	AO	Differential data 2 pair	Always available
MIPI_DSI0_LN2_N	184	AO		
MIPI_DSI0_LN3_P	170	AO	Differential data 3 pair	Always available
MIPI_DSI0_LN3_N	172	AO		

4.3 Camera Interface

CM-QS600 Camera interfaces are derived from the APQ8064 MIPI CSI subsystem. CM-QS600 features a one 4 lane MIPI-CSI interface for a primary camera. PHY block provides physical interface to camera sensor. The following main features are supported:

- Maximum data rate of 1Gbps per lane
- Supported input formats
  - Bayer RGB
  - YCbCr 4:2:2 interleaved
  - 12-8, 12-6, 10-8, 10-6 MIPI compression
  - 8/10/12 MIPI raw

Table 10 MIPI Camera Interface signals

Signal Name	Pin #	Type	Description	Availability
Primary camera serial interface				
MIPI_CSI0_LANE0_P	83	AI	Differential data positive input	Always available
MIPI_CSI0_LANE0_N	85	AI	Differential data negative input	Always available
MIPI_CSI0_LANE1_P	89	AI	Differential data positive input	Always available
MIPI_CSI0_LANE1_N	91	AI	Differential data negative input	Always available
MIPI_CSI0_LANE2_P	93	AI	Differential data positive input	Always available
MIPI_CSI0_LANE2_N	95	AI	Differential data negative input	Always available
MIPI_CSI0_LANE3_P	113	AI	Differential data positive input	Always available
MIPI_CSI0_LANE3_N	115	AI	Differential data negative input	Always available
CLK_500M_MIPI_CSI0_P	107	AO	Differential clock positive input	Always available
CLK_500M_MIPI_CSI0_N	109	AO	Differential clock negative input	Always available

4.4 Audio Subsystem

The following audio interfaces are available with CM-QS600:

- Analog audio interface, including stereo in, stereo out and an analog microphone (Optional)
- I2S compliant digital audio interface.
- HDMI Audio.

4.4.1 Analog Audio CODEC

The CM-QS600 analog audio functionality is implemented by interfacing the Qualcomm WCD9311 audio codec with APQ8064 SLIMbus interface. The Qualcomm WCD9311 supports the following features:

Rx processing features

- Dedicated ADC for each analog input
- MBHC with dedicated input to the ADC
- 100 dB signal-to-noise ratio (SNR) (minimum) with 2.2 V analog supply and 0 dB gain mode
- Input programmable gain settings of 0, 6, 12, and 18 dB
- Three independent pulse-code modulation (PCM) rates to support voice, music, and ultrasonic rates concurrently
- Sample rates of 8, 16, 32, 48, 96, and 192 kHz
- 2 mW stereo record at 48 kHz sample rate
- Digital gain control from -80 to +40 dB in 0.5 dB increments, plus mute

Tx processing features

- Eight analog outputs – earpiece, headphone left and right, and five line outputs
- Eight DACs and seven interpolation paths (earpiece and headphone-left share one DAC path)
- 110 dB (typical) headphone SNR
- Stereo single-ended headphone outputs (16 or 32 Ω): Capless, class G, 63 mW into 16 Ω (each)
- Five single-ended line outputs (600 Ω)
- Auxiliary programmable gain amplifier (PGA) to DAC PA mixing on all analog outputs, plus stereo to mono mixing
- 4 mW stereo playback at a 48 kHz sample rate

- Sample rates of 8, 16, 32, 48, 96, and 192 kHz

For more information please refer to WCD9311 Device Specification 80-N1764-1 document

Table 11 Analog Audio Characteristics

Parameter		Comments	Min	Typ	Max	Unit
Stereo Headphone Output - 8 kHz; 16 bits						
Receive noise		A-weighted; input = -999 dBFS		4.5	6.0	uVrms
SNR		Ratio of full-scale output to output noise level	101	102.5		dB
THD + N	PCMI=-1 dBFS	Band-limited from 200Hz to 20 kHz	68	72		dB
	PCMI=-60 dBFS		36	38		
Stereo Headphone Output - 48 kHz; 16 bits						
Receive noise		A-weighted; input = -999 dBFS		4.5	6.0	uVrms
SNR		Ratio of full-scale output to output noise level	101	102.5		dB
THD + N	PCMI=-1 dBFS	Band-limited from 200Hz to 20 kHz	84	89		dB
	PCMI=-60 dBFS		38	40		
Stereo Headphone Output - 48 or 192 kHz; 24 bits						
Receive noise		A-weighted; input = -999 dBFS		4.5	6.0	uVrms
SNR		Ratio of full-scale output to output noise level	101	102.5		dB
THD + N	PCMI=-1 dBFS	Band-limited from 200Hz to 20 kHz	84	89		dB
	PCMI=-60 dBFS		38	44		
Stereo Headphone Output - Other characteristics						
Full-scale output voltage		f = 1.02 kHz, 0 dB FS; 16 Ω load	0.65	0.69	0.73	Vrms
Output power f = 1.02 kHz, 0 dB FS		16 Ω load	26.4	29.7	33.3	mW
		32 Ω load	25.8	29.4	33.1	
Output load		16 Ω nominal	13	16	50000	Ω
		32 Ω nominal	26	32	50000	
Power supply rejection:	0 kHz < f < 1 kHz	100 mVpp squarewave imposed on power supply; digital input = -999 dBFS	80	90		dB
	1 kHz < f < 5 kHz		70	80		
	5 kHz < f < 20 kHz		60	70		
Output DC offset			-0.81	0	0.81	mV
Line Input to ADC						
Full-scale input voltage			-0.5	0	0.5	dBv
Absolute gain error		-20 dBv input level, 1.02 kHz	-0.5		0.5	dB
Power supply rejection:	0 kHz < f < 1 kHz	100 mVpp square wave imposed on power supply; analog input = 0 Vrms	51	56		dB
	1 kHz < f < 5 kHz		51	56		
	5 kHz < f < 20 kHz		51	56		
Interchannel isolation		20 < f < 20 kHz; IN_1 terminated with 1 k Ω; IN_2 = -5 dBFS at 1 kHz	90	100		dB
Rx to Tx cross-talk attenuation		Tx path measurement with -5 dBFS Rx path signal. f = 1 kHz	90	100		dB
Mute attenuation		0dB, 1 kHz input tone		80		dB
Input resistance		All gain modes	16	20	24	kΩ
Input capacitance				15		pF
Microphone Input to ADC						
Input referred noise				9.2	11.5	uVrms
SNR			90	93		dB
Dynamic range, (see Note 3)		A-weighted, −60-dB full-scale input		85		dB
Total harmonic distortion		Input level = -1 dBV		86	91	dB
		Input level = -60 dBV		34	41	
Microphone Bias						
Bias voltage			1.7		2.85	V

Parameter	Comments	Min	Typ	Max	Unit
Bias-current source				3	mA
Output noise	0.1 µF bypass	0.5	2.0	3.0	uVrms

Table 12 Analog Audio signals

Signal Name	Pin #	Type	Description	Availability
CDC_HPH_RM	201	AO	Right channel headphone output	Only with "**A**" option
CDC_HPH_LP	203	AO	Left channel headphone output	Only with "**A**" option
CDC_IN6_P	197	AI	Right channel line input	Only with "**A**" option
CDC_IN5_P	199	AI	Left channel line input	Only with "**A**" option
CDC_IN2_P	193	AI	Microphone input	Only with "**A**" option
CDC_MIC_BIAS2	191	AP	Electret microphone bias supply	Only with "**A**" option

NOTE: Analog audio codec and interface are only available with the 'A' configuration option.

4.4.2 Digital Audio Interfaces

4.4.2.1 Audio I2S interface – speaker output

- Compliant with the Philips I2S bus specifications
- Supports these sample rates: 8, 16, 32, 48, 96, and 192 kHz
- Support for 8, 12, 16, 20, 24 and 32 bit data sizes.

Table 13 I2S signals

Signal Name	Pin #	Type	Description	Availability
I2S2_MCLK	185*	O	Speaker codec I2S master clock	Always available
SPKR_I2S_DOUT	139*	O	Speaker codec I2S data output	Always available
I2S2_WS	145*	IO	Speaker codec I2S word select	Always available
I2S2_SCK	137*	IO	Speaker codec I2S bit clock	Always available

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.6 of this document.

4.4.2.2 Audio I2S interface – microphone input

- Compliant with the Philips I2S bus specifications
- Supports these sample rates: 8, 16, 32, 48, 96, and 192 kHz
- Support for 8, 12, 16, 20, 24 and 32 bit data sizes.

Table 14 I2S signals

Signal Name	Pin #	Type	Description	Availability
MIC_I2S_MCLK	129*	O	Speaker codec I2S master clock	Always available
MIC_I2S_DIN	163*	O	Speaker codec I2S data output	Always available
MIC_I2S_WS	135*	IO	Speaker codec I2S word select	Always available
MIC_I2S_SCK	161*	IO	Speaker codec I2S bit clock	Always available

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.6 of this document.

4.5 WLAN and Bluetooth

CM-QS600 features 802.11b/g/n and Bluetooth 4.0 wireless connectivity solution, implemented by interfacing the Qualcomm QCA6234X WLAN + Bluetooth combo controller module with the APQ8064 WLSDIO (SDC-4) interface.

Two stream (2x2) 802.11n provides highest throughput and superior RF performance for handheld devices:

- 40MHz channels at 5GHz
- Half Guard Interval for high throughput
- Frame Aggregation for high throughput
- Space Time Block Coding (STBC) Rx for improved downlink robustness over range
- Low Density Parity Check (LDPC) encoding for improved uplink and downlink robustness over range
- Maximum Ratio Combining (MRC)
- Maximum Likelihood (ML) Decoder
- Frame Aggregation (A-MPDU) processing
- De-capsulation of the 802.11 frame to 802.3 frame
- Bluetooth low energy (BT4.0) ready
- Class 1.5 Bluetooth with integrated Tx/Rx switch.
- Bluetooth and cell phone(GSM/DCS/WCDMA/UMTS/3G) co-existence

Additional features:

- All WLAN RF transmitters are pre-calibrated
- Near zero power consumption in idle and stand-by enables users to leave WLAN and BT "always on."
- Advanced BT/WLAN coexistence and concurrent RX for superior rate-over-range and very low latency
- Best in class Rx sensitivity for superior throughput rate-over-range performance
- Integrated Sleep Clock eliminates the need for expensive bulky 32 KHz real-time clock
- Integrated conformal RF shielding and near-zero RBOM for lowest cost

Antenna Connection

QCA6234X requires two 2.4GHz antennas for dual band WiFi & Bluetooth. The antennas are connected via the on-board UFL high frequency connector J2 and J3. Any type of 2.4GHz antenna can be used. Please refer to section 6.3 for connector location.

Table 15 J2 and J3 connector data

Manufacturer	Mfg. P/N	Mating Connector
Hirose	U.FL-R-MT(10)	Hirose U.FL-LP-040

Table 16 802.11b/g (WLAN) RF system specifications

To be added in a later revision of this document.

NOTE: The WLAN and Bluetooth module is available only with the 'WB' configuration option.

4.6 PCIe

The CM-QS600 supports a x1 PCIe 2.0 link. The PCIe interface is derived directly from APQ8064 SoC. The PCI Express module in APQ8064 SoC does not generate the PCI Express ref clock differential signal. The CM-QS600 overcomes this limitation by driving a clock from external PCIe 2.0 clock generator.

Signal Name	Pin #	Type	Description	Availability
CLK_100M_EDGE_PCIE_CLK_P	119	AO	Differential clock pair	Only without "**E**" option
CLK_100M_EDGE_PCIE_CLK_N	121	AO		Only without "**E**" option
C_CPU_PCIE_TX_P_C	125	AO	Differential transmit data pair	Only without "**E**" option
C_CPU_PCIE_TX_N_C	127	AO		Only without "**E**" option
CPU_PCIE_RX_P_C	131	AI	Differential receive data pair	Only without "**E**" option
CPU_PCIE_RX_N_C	133	AI		Only without "**E**" option

4.7 Ethernet

CM-QS600 incorporates a full-featured Gigabit Ethernet interface. The interface is implemented with Atheros AR8151-B controller connected to the APQ8064 PCIe interface.

The CM-QS600 Ethernet interface supports the following main features:

- Integrated PHY for 10/100/1000 Mbps
- IEEE 802.3 Auto-Negotiation support.
- IEEE 802.3ab PHY compliance and compatibility
- Supports automatic MDI/MDIX functions
- Cable Diagnostic Test (CDT) for open, short cable, cable length detection, and incorrect or mismatched impedance
- IEEE 802.3az support
- IEEE 802.3x compliant flow control support
- Interrupt coalescing
- PHY support for HP Auto-MDIX
- Activity and speed indicator LED controls
- Descriptor ring management for Tx/Rx
- IPv4 and IPv6 support
- 802.3u support
- IEEE 802.1Q VLAN feature
- Jumbo frame support
- Automatic polarity correction
- Media Access Control

Table 17 Ethernet interface signals

Signal Name	Pin #	Type	Description	Availability
ETH_TRX0_P	8	AIO	Media dependent interface 0	Only with "**E**" option
ETH_TRX0_N	6	AIO		Only with "**E**" option
ETH_TRX1_P	14	AIO	Media dependent interface 1	Only with "**E**" option
ETH_TRX1_N	12	AIO		Only with "**E**" option
ETH_TRX2_P	20	AIO	Media dependent interface 2	Only with "**E**" option
ETH_TRX2_N	18	AIO		Only with "**E**" option
ETH_TRX3_P	26	AIO	Media dependent interface 3	Only with "**E**" option

ETH_TRX3_N	24	AIO		Only with "**E**" option
V1P7_ETH_VDDCT	2	AP	Magnetics central TAP voltage	Only with "**E**" option
ETH_LED0	16	O,PU	Driven low when link is detected. When link activity is detected, drives high pulse (80mS).	Only with "**E**" option
ETH_LED1	4	O,PU	Driven low when link speed is 100Mbps, Driven high during 10Mbps operation or during line isolation.	Only with "**E**" option
ETH_LED2	22	O,PU	Driven low when full duplex operation is detected.	Only with "**E**" option

NOTE: For magnetics selection recommendations, please refer to section 8.3 of this document.

4.8 USB interfaces

4.8.1 USB 2.0 On-The-Go

The USB 2.0 OTG interface is implemented with the APQ8064 USB OTG subsystem with built-in PHY.

- USB2.0 peripheral (function controller) in full and high speed (12 and 480 Mbps respectively)
- USB2.0 host in low, full and high-speed (1.5, 12 and 480 Mbps respectively) with one downstream port with split transaction support (allows multiple ports through a hub).

CM-QS600 implementation of the USB2.0 OTG interface allows a CM-QS600 based system to boot upon USB power source connection, draw system power from USB and charge the main battery from USB (appropriate circuitry such as charger must be implemented on carrier board). For additional information please refer to chapter 5.2.3 and 5.5 of this document.

Please refer to APQ8064 reference manual for detailed information on the USB3 controller and PHY.

Table 18 USB 2.0 OTG interface signals

Signal Name	Pin #	Type	Description	Availability
CPU_USB1_D_P	176	AIO	USB2.0 OTG positive data	Always available
CPU_USB1_D_N	178	AIO	USB2.0 OTG negative data	Always available
USB1_ID	174	AIO	USB OTG ID signal	Always available
V5_OTG	180	P	VBUS Power input/output/sense. When USB-OTG is in HOST mode, CM-QS600 sources 5V (up to 500mA) at this pin. When USB-OTG is in DEVICE mode, CM-QS600 draws VBUS power from the USB host through this pin. **NOTE: CM-QS600 can change power state upon voltage sensed through this pin. If not used, leave NC**	Always available

4.8.2 USB 2.0 Host

The CM-QS600 high-speed USB interface is implemented with APQ8064 USB 2.0 subsystem. The USB system supports the following main features:

- Two USB 2.0 High Speed (480Mbps) compatible downstream ports
- Supports either Single-TT or Multi-TT configurations for Full-Speed (12Mbps) and Low-Speed (1.5Mbps) connections

Please refer to APQ8064 datasheet for additional information.

Table 19 USB 2.0 Host interface signals

Signal Name	Pin #	Type	Description	Availability
Host Port-3				
CPU_USB3_D_P	160	AIO	USB host port 2 positive data	Always available
CPU_USB3_D_N	158	AIO	USB host port 2 negative data	Always available
Host Port-4				
CPU_USB4_D_P	166	AIO	USB host port 3 positive data	Always available
CPU_USB4_D_N	164	AIO	USB host port 3 negative data	Always available

4.9 GSBI

GSBI ports are connectivity ports that can function as UART, SPI, I2C or GPIO. CM-QS600 features up to five GSBI ports. Each port is four bits wide: GSBIx_[3:0] and can be configured by software

Table 20 GSBI Options

#	Configuration	GSBI bit 3	GSBI bit 2	GSBI bit 1	GSBI bit 0
GSBI1 GPIO pins = GSBI2 GPIO pins = GSBI3 GPIO pins = GSBI4 GPIO pins = GSBI5 GPIO pins = GSBI6 GPIO pins = GSBI7 GPIO pins =		GPIO_18 GPIO_22 GPIO_6 GPIO_10 GPIO_51 GPIO_14 GPIO_82	GPIO_19 GPIO_23 GPIO_7 GPIO_11 GPIO_52 GPIO_15 GPIO_83	GPIO_20 GPIO_24 GPIO_8 GPIO_12 GPIO_53 GPIO_16 GPIO_84	GPIO_21 GPIO_25 GPIO_9 GPIO_13 GPIO_54 GPIO_17 GPIO_85
1	4-pin UART	UART_TX O	UART_RX I	UART_CTS I	UART_RFR O
2	4-pin SPI	SPI_DATA_MOSI IO	SPI_DATA_MISO IO	SPI_CS_N IO	SPI_CLK IO
3	3-pin UIM + 1 GPIO	UIM_DATA IO UIM data	UIM_CLK O UIM clock	UIM_RESET_N O UIM reset	GPIO_XX IO Configurable I/O
4	2-pin I2C + 2-pin UART	UART_TX O 2-pin UART TX	UART_RX I 2-pin UART RX	I2C_SDA IO I2C serial data	I2C_SCL IO I2C serial clock
5	UIM + I^2C	UIM_DATA IO UIM data	UIM_CLK O UIM clock	I2C_SDA IO I2C serial data	I2C_SCL IO I2C serial clock
6	4 GPIOs	GPIO_XX	GPIO_XX IO	GPIO_XX IO	GPIO_XX IO

4.10 UARTs

Up to 5 UART ports are available with CM-QS600. All the UART ports are derived from the APQ8064 SoC GSBI ports and support the following features:

- High-speed UART operation up to 4 Mbps and medium data-rate IrDA operation up to 1.152 Mbps.
- Applicable standard: EIA RS232-C
- Rate-controlled data mover with separate CRCI channels for Rx and Tx
- Larger Rx and Tx FIFOs that are implemented in one SRAM
- Access to the fast peripheral bus (32-bit wide AHB interface) rather than the slow bus

Table 21 UART signals

Signal Name	Pin #	Type	Description	Availability
UART-2				
UART2_TX	3*	O	UART-2 serial data transmit	Always available
UART2_RX	5*	I	UART-2 serial data receive	Always available
UART2_CTS	7*	O	UART-2 clear to send.	Always available

Signal Name	Pin #	Type	Description	Availability
UART2_RTS	9*	I	UART-2 request to send.	Always available
UART-3				
UART3_TX	65*	O	UART-3 serial data transmit	Always available
UART3_RX	63*	I	UART-3 serial data receive	Always available
UART3_CTS	58*	O	UART-3 clear to send.	Always available
UART3_RTS	69*	I	UART-3 request to send	Always available
UART-4				
UART4_TX	70*	O	UART-4 serial data transmit	Always available
UART4_RX	72*	I	UART-4 serial data receive	Always available
UART4_CTS	68*	O	UART-4 clear to send.	Always available
UART4_RTS	66*	I	UART-4 request to send	Always available
UART-5				
UART5_TX	163*	O	UART-5 serial data transmit	Always available
UART5_RX	129*	I	UART-5 serial data receive	Always available
UART5_CTS	155*	O	UART-5 clear to send.	Always available
UART5_RTS	161*	I	UART-5 request to send.	Always available
UART-6				
UART6_TX	60*	O	UART-6 serial data transmit	Without "**WB**" option
UART6_RX	62*	I	UART-6 serial data receive	Without "**WB**" option
UART6_CTS	49*	O	UART-6 clear to send.	Without "**WB**" option
UART6_RTS	43*	I	UART-6 request to send.	Without "**WB**" option
UART-7				
UART7_TX	117	O	UART-7 serial data transmit	Always available
UART7_RX	111	I	UART-7 serial data receive	Always available

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.6 of this document.

UART 7 is a debug serial interface

4.11 MMC / SD / SDIO

The CM-QS600 features 3 MMC / SD / SDIO host interfaces implemented with the APQ8064 integrated MMC/SDIO host controller modules. The following main features are supported by MMC/SDIO modules:

- Clock output up to 104 MHz on SDC2, up to 208 MHz on SDC3 and up to 67 MHz on the SDC4
- 2.95 V voltage operation on SDC3; 1.8 V operation on SDC2 and SDC4
- Support for SDIO host mode
- SDIO-compatible WLAN (802.11)
- Interface with SD/MMC memory cards up to 2 TB
- 10k pull-up resistor on command pin; placeholder pullups are recommended on the data lines also.

Each MMC/SD/SDIO host controller can support a single MMC / SD / SDIO card or device.

Table 22 SDC controller parameters

SDC	Max. Clock rate	Width	MMC standard	SD standard
SDC2	104 MHz SDR	4 bits	MMC 4.4 type 3 SDR	UHS-SDR50
SDC3	52 MHz DDR	4 bits	MMC 4.4 type 3 SDR	UHS-SDR104
SDC4	52 MHz SDR	4 bits	MMC 4.4 type 3 SDR	UHS-SDR50

Table 23 MMC / SD / SDIO signals

Signal Name	Pin #	Type	Description	Availability
SDC-2 (SDCARD)				
SDC2_CLK	157	O	Interface clock	Always available
SDC2_CMD	147	IO	Command signal	Always available
SDC2_DATA_0	155	IO	Card data bit 0	Always available
SDC2_DATA_1	153	IO	Card data bit 1	Always available
SDC2_DATA_2	151	IO	Card data bit 2	Always available
SDC2_DATA_3	149	IO	Card data bit 3	Always available
SDC-3 (SDCARD)				
CLK_208M_SDC3	80	O	Interface clock	Always available
SDC3_CMD	82	IO	Command signal	Always available
SDC3_DATA_0	84	IO	Card data bit 0	Always available
SDC3_DATA_1	86	IO	Card data bit 1	Always available
SDC3_DATA_2	88	IO	Card data bit 2	Always available
SDC3_DATA_3	90	IO	Card data bit 3	Always available
SDC3_WP	67*	O	Write protect	Always available
SDC3_CD	61*	I	Card detect	Always available
SDC-4 (WLSDIO)				
CLK_54M_WLAN_SD	54	O	Interface clock	Without "**WB**" option
SDC4_CMD	56	IO	Command signal	Without "**WB**" option
SDC4_ DATA_0	11	IO	Card data bit 0	Without "**WB**" option
SDC4_ DATA_1	13	IO	Card data bit 1	Without "**WB**" option
SDC4_ DATA_2	15	IO	Card data bit 2	Without "**WB**" option
SDC4_ DATA_3	17	IO	Card data bit 3	Without "**WB**" option

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.6 of this document.

4.12 GPIO

Up to 82 GPIO signals are available with CM-QS600. Most of the available GPIOs are derived from the APQ8064 integrated General-Purpose Interface and additional signal are derived from the PMM8920 PMIC.

Please refer to APQ8064 reference manual for detailed information on the integrated General-Purpose Interface.

NOTE: Not all GPIO signals supported by the APQ8064 SoC are available through the CM-QS600 carrier board interface.

Table 24 GPIO availability

Signal name	Pin #	Type	Availability	Notes
CPU_GPIO_22	3*	IO	Always available	GSBI2
CPU_GPIO_23	5*	IO	Always available	GSBI2
CPU_GPIO_24	7*	IO	Always available	GSBI2
CPU_GPIO_25	9*	IO	Always available	GSBI2
CPU_GPIO_66	11*	IO	Only without "WB"	
CPU_GPIO_65	13*	IO	Only without "WB"	
CPU_GPIO_64	15*	IO	Only without "WB"	
CPU_GPIO_63	17*	IO	Only without "WB"	
CPU_GPIO_70	25*	IO	Always available	
CPU_GPIO_71	31*	IO	Always available	
CPU_GPIO_17	43*	IO	Only without "WB"	GSBI6
CPU_GPIO_16	49*	IO	Only without "WB"	GSBI6
CPU_GPIO_26	61*	IO	Always available	

Signal name	Pin #	Type	Availability	Notes
CPU_GPIO_7	63*	IO	Always available	GSBI3
CPU_GPIO_6	65*	IO	Always available	GSBI3
CPU_GPIO_30	67*	IO	Always available	
CPU_GPIO_9	69*	IO	Always available	GSBI3
CPU_GPIO_27	73*	IO	Always available	
CPU_GPIO_82	111*	IO	Always available	GSBI7
CPU_GPIO_83	117*	IO	Always available	GSBI7
CPU_GPIO_54	129*	IO	Always available	GSBI5
CPU_GPIO_53	135*	IO	Always available	GSBI5
CPU_GPIO_47	137*	IO	Always available	GSBI5
CPU_GPIO_49	139*	IO	Always available	
CPU_GPIO_56	143*	IO	Always available	
CPU_GPIO_48	145*	IO	Always available	
CPU_GPIO_57	147*	IO	Always available	
CPU_GPIO_58	149*	IO	Always available	
CPU_GPIO_60	151*	IO	Always available	
CPU_GPIO_61	153*	IO	Always available	
CPU_GPIO_62	155*	IO	Always available	
CPU_GPIO_59	157*	IO	Always available	
CPU_GPIO_52	161*	IO	Always available	GSBI5
CPU_GPIO_51	163*	IO	Always available	GSBI5
CPU_GPIO_50	185*	IO	Always available	BOOT_CONFIG PIN
CPU_GPIO_1	187*	IO	Always available	
CPU_GPIO_69	34*	IO	Always available	
CPU_GPIO_72	40*	IO	Always available	
CPU_GPIO_29	52*	IO	Always available	
CPU_GPIO_8	58	IO	Always available	GSBI3
CPU_GPIO_14	60*	IO	Only without "WB"	GSBI6
CPU_GPIO_15	62*	IO	Only without "WB"	GSBI6
CPU_GPIO_13	66*	IO	Always available	GSBI4
CPU_GPIO_12	68*	IO	Always available	GSBI4
CPU_GPIO_10	70*	IO	Always available	GSBI4
CPU_GPIO_11	72*	IO	Always available	GSBI4
PMIC_MPP_8921_12	98	IO	Always available	
PMIC_GPIO_30	100*	IO	Always available	
PMIC_MPP_8921_02	102*	IO	Always available	
CPU_GPIO_55	104	IO	Always available	
PMIC_MPP_8921_04	106	IO	Always available	
CPU_GPIO_86	108	IO	Always available	
CPU_GPIO_80	110	IO	Always available	
PMIC_MPP_8921_03	112	IO	Always available	
CPU_GPIO_3	116*	IO	Always available	
PMIC_MPP_8821_3	118	IO	Always available	
CPU_GPIO_28	120*	IO	Always available	
PMIC_PM_GPIO_5	122	IO	Always available	
CPU_GPIO_39	124	IO	Always available	Must be PD with 10K
CPU_GPIO_34	126*	IO	Always available	Must be PD with 10K
CPU_GPIO_33	128*	IO	Always available	Must be PD with 10K
CPU_GPIO_5	130*	IO	Always available	Must be PD with 10K
CPU_GPIO_38	134*	IO	Always available	
CPU_GPIO_37	136*	IO	Always available	
CPU_GPIO_35	142*	IO	Always available	
CPU_GPIO_36	144*	IO	Always available	
PMIC_MPP_8821_11	146	IO	Always available	
CPU_GPIO_84	148	IO	Always available	
CPU_GPIO_31	152*	IO	Always available	
PMIC_MPP_8821_10	154	IO	Always available	
CPU_GPIO_0	156	IO	Always available	
PMIC_MPP_8821_8	198	IO	Always available	
PMIC_MPP_8821_9	200	IO	Always available	
PMIC_MPP_8821_7	202	IO	Always available	

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.6 of this document.

4.13 I²C

CM-QS600 features up to five general purpose I²C interfaces via GSBI ports. The following features are supported:

- Two-wire bus for inter-IC communications supporting any IC fabrication process
- Each device is recognized by a unique address, and can operate as either a transmitter or receiver, depending on the device function
- The I2C controller provides an interface between the CPSS fast peripheral bus (FPB), an advanced high-performance bus (AHB), and the industry-standard I2C serial bus
- It is I2C-compliant, high-speed mode (HS-mode)-compliant, and a master-only device
- Clock speed is 384 kHz
- I2C pins use GPIOs configured as open-drain outputs; the pullup resistor is provided by the slave
- Camera auto-focus control via I2C originates with the aDSP; a separate hardware request port is required at the I2C controller.

Table 25 I²C signals

Signal Name	Pin #	Type	Description	Availability
I²C-2				
I2C2_SDA	7*	SPU/SPD	I²C serial data line	Always available
I2C2_SCL	9*	SPU/SPD	I²C serial clock line	Always available
I²C-3				
I2C3_SDA	58*	SPU/SPD	I²C serial data line	Always available
I2C3_SCL	69*	SPU/SPD	I²C serial clock line	Always available
I²C-4				
I2C4_SDA	68*	SPU/SPD	I²C serial data line	Always available
I2C4_SCL	66*	SPU/SPD	I²C serial clock line	Always available
I²C-5				
I2C5_SDA	163*	SPU/SPD	I²C serial data line	Always available
I2C5_SCL	161*	SPU/SPD	I²C serial clock line	Always available
I²C-6				
I2C6_SDA	49*	SPU/SPD	I²C serial data line	Without "**WB**" option
I2C6_SCL	43*	SPU/SPD	I²C serial clock line	Without "**WB**" option

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.6 of this document.

4.14 SPI

CM-QS600 features up to five SPI ports. All CM-QS600 SPI ports are derived from the APQ8064 GSBI ports. SPI ports support the following main features:

- 4-bit synchronous serial data link.
- Master and slave mode supported
- Up to 52 MHz in both master and slave mode
- Master device initiates data transfers; multiple slave devices are supported by using chip selects
- No explicit communication framing, error checking, or defined data word lengths, so the transfers are strictly at the raw bit level

- As SPI master, the core supports several SPI system configurations (as defined by the SPI protocol):
  - Configurations 1, 2, 4, and 5 are supported, though configurations 4 and 5 are software dependent
  - Configuration 3 and the multi-master configuration are not supported

Table 26 SPI signals

Signal Name	Pin #	Type	Description	Availability
SPI-2				
SPI2_CLK	9*	IO	SPI-2 Master clock out; slave clock in	Always available
SPI2_CS_N	7*	IO	SPI-2 Chip select	Always available
SPI2_MISO	5*	IO	SPI-2 Master data out; slave data in	Always available
SPI2_MOSI	3*	IO	SPI-2 Master data in; slave data out	Always available
SPI-3				
SPI2_CLK	69*	IO	SPI-3 Master clock out; slave clock in	Always available
SPI2_CS_N	58*	IO	SPI-3 Chip select 0	Always available
SPI2_MISO	63*	IO	SPI-3 Master data out; slave data in	Always available
SPI2_MOSI	65*	IO	SPI-3 Master data in; slave data out	Always available
SPI-4				
SPI4_CLK	66*	IO	SPI-4 Master clock out; slave clock in	Always available
SPI4_CS_N	68*	IO	SPI-4 Chip select	Always available
SPI4_MISO	72*	IO	SPI-4 Master data out; slave data in	Always available
SPI4_MOSI	70*	IO	SPI-4 Master data in; slave data out	Always available
SPI-5				
SPI5_CLK	161*	IO	SPI-5 Master clock out; slave clock in	Always available
SPI5_CS_N	163*	IO	SPI-5 Chip select	Always available
SPI5_MISO	129*	IO	SPI-5 Master data out; slave data in	Always available
SPI5_MOSI	135*	IO	SPI-5 Master data in; slave data out	Always available
SPI-6				
SPI6_CLK	43*	IO	SPI-6 Master clock out; slave clock in	Without "**WB**" option
SPI6_CS_N	49*	IO	SPI-6 Chip select	Without "**WB**" option
SPI6_MISO	62*	IO	SPI-6 Master data out; slave data in	Without "**WB**" option
SPI6_MOSI	60*	IO	SPI-6 Master data in; slave data out	Without "**WB**" option

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.6 of this document.

4.15 Touch screen

CM-QS600 provides touch screen support for capacitive panels via external IC (I2C, SPI, and interrupts)

Table 27 Touch screen interface

Signal Name	Pin #	Type	Description	Availability
TS_PENIRQ_N	61*	I	Touch screen pen-down interrupt	Always available
TS_EOC	63*	I	Touch screen end-of-conversion interrupt	Always available
SSBI_TS	65*	IO	Single-wire serial bus interface for touch screen	Always available

NOTE: Pins denoted with "*" are multifunctional. For details, please refer to section 5.6 of this document.

5 SYSTEM LOGIC

5.1 Power Supply

The CM-QS600 supports two power supply options:

- Regulated DC supply (5V typical).
- Lithium-ion polymer battery.

CM-QS600 does not feature an on-board Lithium-ion polymer battery charger. If required, such a charger must be implemented on the carrier board.

Table 28 Power signals

Signal Name	Pin#	Type	Description
V5_SB	10,28,46,64,78,96,114 132,150,168,186	P	Main power supply. Connect to a regulated DC supply (5V Typ.).
V3_COIN	183	P	RTC back-up battery power input. Connect to a 3V coin-cell lithium battery. Use 4.7uF capacitor instead of a coin-cell battery if RTC back-up is not required.
VBAT	192	P	Connect a Lithium-ion polymer battery if desired.
GND	19,37,55,71,87,105 123,141,159,177,195	P	Common ground.

5.2 Power Management

To be added in a later revision of this document.

5.2.1 Power Resources and Control Signals.

To be added in a later revision of this document.

5.2.2 CM-QS600 Operating Modes

CM-QS600 power state is defined by the state of all CM-QS600 power-resources.

The following power states are supported by CM-QS600 (derived from PMM8920 power states)

Table 29 CM-QS600 Power States

CM-QS600 Static mode	Enabling signals	Mode description
Active	Valid main battery (VBAT > 2.5) or external supply (5V_SB > 4.5V)	Normal operating mode for PMM8920 Default-on regulators on (and others as desired) VREF circuit on in its normal mode Crystal oscillator and XO buffers on All other functions controlled individually via SBI
Sleep	Valid main battery or external supply SBI functional, disables most PM circuits	Power-saving mode for PMM8920 Key regulators on in their low-power modes VREF circuit on in its low-power mode Crystal oscillator on, XO buffers off Other circuits controlled individually via SBI, and are typically disabled for minimum power dissipation
Off1	Valid main battery SBI not functional	Device almost fully off, powered by main battery Crystal oscillator and RTC circuits are enabled All other functions and regulators are disabled

CM-QS600 Static mode	Enabling signals	Mode description
Off2	Valid coin-cell only SBI not functional	Device almost completely turned off, powered by coin-cell Crystal oscillator and RTC circuits are enabled All other functions and regulators are disabled
Off3	Valid coin-cell or backup capacitor SBI not functional	Device completely turned off Crystal oscillator and RTC circuits are disabled All other functions and regulators are disabled

5.2.3 Power-On and Power-Off

CM-QS600 first boot sequence (first transition from OFF to ACTIVE state) starts as soon as V5_SB or VBAT rail receives their valid voltage levels.

5.2.3.1 ON, OFF and gating signals active by default

The following signals are sources of ON, OFF and gating conditions by default

Table 30 ON, OFF and Gating signals active by default

Signal Name	Pin #	Type	Description	Availability
RSTBTN#	171	I	Active Low cold reset input signal. If Asserted, serves as an ON Gating condition.	Always available
PWRBTN#	165	I	Pulled-Up Active low PWRON signal (designed for an ON/OFF switch). ON and OFF requests can be triggered upon voltage sensed through this signal. NOTE: leave floating if not used.	Always available
VBAT	192		TBD	
V5_OTG	180	AI	TBD	Always available
V5_SB	10,28,46,64,78,96,114 132,150,168,186	P	Main system power input and sense. If V5_SB voltage is too low (<4.5V), serves as an ON Gating condition	Always available

5.3 Reset

CM-QS600 supports cold reset signal (RSTBTN#)

- Cold reset is an input to the PMM8920, which triggers a full logic reset to CM-QS600. Cold reset is a global reset that affects every module on the device.

The COLD_RESET_IN signal should be used as the main system reset.

Table 31 Reset signals

Signal Name	Pin #	Type	Description	Availability
COLD_RESET_IN	171	I	Active Low cold reset input signal. Should be used as main system reset	Always available

5.4 Boot Sequence

CM-QS600 boot sequence defines which interface/media is used by CM-QS600 to load and execute the initial software (such as U-boot). CM-QS600 can load initial software from following interfaces/media:

- On-board eMMC device (SDC1).
- External SD/MMC card using the SDC-3 interface.

CM-QS600 will query boot devices/interfaces for initial software in the order defined by the active boot sequence. A total of two different boot sequences are supported by CM-QS600:

- Standard sequence: Designed for normal system operation with the on-board eMMC device as the boot media.
- Alternate sequence: Designed to bypass the eMMC device. Using the alternate sequence allows CM-QS600 to boot from external SD card, effectively bypassing the onboard eMMC.

The initial logic value of ALT_BOOT signal defines which of the supported boot sequences is used by the system.

Table 32 Alternative Boot selection signal

Signal Name	Pin #	Type	Description	Availability
ALT_BOOT	185	I	Boot sequence selector signal. Pull high for standard boot sequence.	Always available

Table 33 CM-QS600 Boot sequences

Boot sequence	ALT_BOOT	First device	Second device
Standard	High	Onboard eMMC	N/A
Alternate	Low	External SDC-3 Drive	Onboard eMMC

5.5 Battery and Charger signals

CM-QS600 can be used as part of a battery powered device. The signals described in this section define system behavior in some of the special cases that apply to battery powered devices.

Using USB wall adapters to recharge the main battery is a very common approach. In many cases, effective battery charging is possible only while the system is active (after boot). Charging the battery in a scenario where the main battery is fully discharged and the system is powered off must be taken into consideration. While CM-QS600 requires more than 100mA current for successful boot, the USB specification limits initial current from a USB host (before USB device initialization) to 100mA.

Table 34 Battery charger related signals

Signal Name	Pin #	Type	Description	Availability
PMIC_BAT_THERM	167	AI	Battery thermistor input	Always available
PMIC_BAT_ID	169	AI	Battery ID input	Always available
PMIC_BMS_CSN	183	AI	Battery current sense – minus. Must be connected to GND if only regulated power supply used.	Always available
PMIC_BMS_CSP	181	AI	Battery current sense – plus. Must be connected to GND if only regulated power supply used.	Always available
VBAT	192	P,AIO	Battery sense input; trickle charge output	Always available
PMIC_ATC_LED_SRC	92	AO	Auto-trickle charge indicator LED supply	Always available

5.6 Signal Multiplexing Characteristics

Up to 30 of the CM-QS600 carrier board interface pins are multifunctional. Multifunctional pins enable extensive functional flexibility of the CM-QS600 CoM by allowing usage of a single carrier board interface pin for one of several functions. Up-to 3 functions (ALT modes) are accessible through each multifunctional carrier board interface pin. The multifunctional capabilities of CM-QS600 pins are derived from the APQ8064 SoC control module.

NOTE: Pin function selection is controlled by software.

NOTE: Each pin can be used for a single function at a time.

NOTE: Only one pin can be used for each function (in case a function is available on more than one carrier board interface pin).

NOTE: An empty ALT mode must be considered as a "RESERVED" function and must not be used.

Table 35 Multifunctional Signals

Pin #	ALT1	ALT2	ALT3	Availability
11	SDC4_DATA_0	GPIO_66	WLAN_DATA_0	Without "WB" option
13	SDC4_DATA_1	GPIO_65	WLAN_DATA_1	Without "WB" option
15	SDC4_DATA_2	GPIO_64	WLAN_DATA_2	Without "WB" option
17	SDC4_DATA_3	GPIO_63	SSBI_BT	Without "WB" option
25	HDMI_DDC_CLK	GPIO_70		
31	HDMI_DDC_DATA	GPIO_71		
34	HDMI_CEC	GPIO_69		
40	HDMI_HPD	GPIO_72		
43	GSBI6_0	BT_DATA_STROBE		Without "WB" option
49	GSBI6_1	BT_CTL		Without "WB" option
54	SDC4_CLK	WLAN_CLK	GPIO_68	Without "WB" option
56	SDC4_CMD	WLAN_CMD	GPIO_67	Without "WB" option
61	SDC3_CD	TS_PENIRQ_N	GPIO_26	
63	GSBI3_2	TS_EOC		
65	GSBI3_3	SSBI_TS		
67	SDC3_WP	GPIO_1		
73	MI2S_WS	GPIO_27		
74	CDC_MIC_I2S_WS	GPIO_36		
75	MI2S_SD2	GPIO_30		
129	GSBI5_0	MIC_I2S_MCLK		
135	GSBI5_1	MIC_I2S_WS		
139	SPKR_I2S_DOUT	GPIO_49		
145	SPKR_I2S_SCK	GPIO_47		
147	SDC2_CMD	GPIO_57		
149	SDC2_DATA_3	GPIO_58		
151	SDC2_DATA_2	GPIO_60		
153	SDC2_DATA_1	GPIO_61		
155	SDC2_DATA_0	GPIO_62		
157	SDC2_CLK	GPIO_59		
161	GSBI5_2	MIC_I2S_SCK		
163	GSBI5_3	MIC_I2S_DIN		

5.7 RTC

The CM-QS600 RTC is implemented with the internal RTC of the APQ8064 SoC. The RTC provides time and calendar information.

Additionally, a backup battery can keep the RTC running to maintain clock and time information even if the main supply is not present. If the backup battery is rechargeable, the device also provides a backup battery charger so it can be recharged when the main battery supply is present. The backup battery should be connected to the V3_COIN power input. If the backup battery is not used in the design, connect this pin to 4.7uF capacitor.

NOTE: VCC_RTC must remain valid at all times for proper operation of the on-board RTC.

6 CARRIER BOARD INTERFACE

The CM-QS600 connects to the carrier board a SODIMM-204 edge connector.

6.1 Connector Pinout

Table 36 Connector P1

Pin #	CM-QS600 Signal Name	Reference Section		Pin #	CM-QS600 Signal Name	Reference Section
1	GND			2	V1P7_ETH_VDDCT	
3	GSBI2_3			4	ETH_LED1	
5	GSBI2_2			6	ETH_TRX0_N	
7	GSBI2_1			8	ETH_TRX0_P	
9	GSBI2_0			10	V5_SB	
11	SDC4_DATA_0 CPU_GPIO_66 WLAN_DATA_0			12	ETH_TRX1_N	
13	SDC4_DATA_1 CPU_GPIO_65 WLAN_DATA_1			14	ETH_TRX1_P	
15	SDC4_DATA_2 CPU_GPIO_64 WLAN_DATA_2			16	ETH_LED0	
17	SDC4_DATA_3 CPU_GPIO_63 SSBI_BT			18	ETH_TRX2_N	
19	GND			20	ETH_TRX2_P	
21	SATA_TX_P			22	ETH_LED2	
23	SATA_TXM			24	ETH_TRX3_N	
25	HDMI_DDC_CLK CPU_GPIO_70			26	ETH_TRX3_P	
27	SATA_RXP			28	V5_SB	
29	SATA_RXM			30	CLK_165M_HDMI_P	
31	HDMI_DDC_DATA CPU_GPIO_71			32	CLK_165M_HDMI_N	
33	LVDS_CLK0_P			34	HDMI_CEC GPIO_69	
35	LVDS_CLK0_N			36	HDMI_TX0_P	
37	GND			38	HDMI_TX0_N	
39	LVDS_TX0_P			40	HDMI_HPLUG_DET GPIO_72	
41	LVDS_TX0_N			42	HDMI_TX1_P	
43	GSBI6_0 BT_DATA_STROBE			44	HDMI_TX1_N	
45	LVDS_TX1_P			46	V5_SB	
47	LVDS_TX1_N			48	HDMI_TX2_P	
49	GSBI6_1 BT_CTL			50	HDMI_TX2_N	
51	LVDS_TX2_P			52	CPU_GPIO_29 MI2S_SD3	
53	LVDS_TX2_N			54	SDC4_CMD WLAN_CMD GPIO_67	
55	GND			56	SDC4_CLK WLAN_CLK GPIO_68	
57	LVDS_TX3_P			58	GSBI3_1	
59	LVDS_TX3_N			60	GSBI6_3	
61	TS_PENIRQ_N CPU_GPIO_26 SDC3_CD			62	GSBI6_2	
63	GSBI3_2 TS_EOC			64	V5_SB	

Pin #	CM-QS600 Signal Name	Reference Section		Pin #	CM-QS600 Signal Name	Reference Section
65	GSBI3_3 SSBI_TS			66	GSBI4_0	
67	CPU_GPIO_1 SDC3_WP			68	GSBI4_1	
69	GSBI3_0			70	GSBI4_3	
71	GND			72	GSBI4_2	
73	CPU_GPIO_27 MI2S_WS			74	CLK_170M_1_LVDS_P	
75	LVDS_TX4_P			76	CLK_170M_1_LVDS_N	
77	LVDS_TX4_N			78	V5_SB	
79	LVDS_TX5_P			80	SDCARD_CLK	
81	LVDS_TX5_N			82	SDC3_CMD	
83	MIPI_CSI0_LANE0_P			84	SDC3_DATA_0	
85	MIPI_CSI0_LANE0_N			86	SDC3_DATA_1	
87	GND			88	SDC3_DATA_2	
89	MIPI_CSI0_LANE1_P			90	SDC3_DATA_3	
91	MIPI_CSI0_LANE1_N			92	PMIC_LED_DRV0_N	
93	MIPI_CSI0_LANE2_P			94	PMIC_ATC_LED_SRC	
95	MIPI_CSI0_LANE2_N			96	V5_SB	
97	LVDS_TX6_P			98	PMIC_MPP_8921_12	
99	LVDS_TX6_N			100	PMIC_GPIO_30 UIM1_CLK	
101	LVDS_TX7_P			102	PMIC_MPP_8921_02 UIM1_DATA	
103	LVDS_TX7_N			104	CPU_GPIO_55	
105	GND			106	PMIC_MPP_8921_04	
107	CLK_500M_MIPI_CSI0 _P			108	CPU_GPIO_86	
109	CLK_500M_MIPI_CSI0 _N			110	CPU_GPIO_80	
111	DEBUG_UART_TXD			112	PMIC_MPP_8921_03	
113	MIPI_CSI0_LANE3_P			114	V5_SB	
115	MIPI_CSI0_LANE3_N			116	CPU_GPIO_3 WDOG_DISABLE	
117	DEBUG_UART_RXD			118	PMIC_MPP_8821_3	
119	PCIE_CLK_P			120	CPU_GPIO_28 MI2S_SCK	
121	PCIE_CLK_N			122	PMIC_PM_GPIO_5	
123	GND			124	CPU_GPIO_39	
125	PCIE_TX+			126	CPU_GPIO_34	
127	PCIE_TX-			128	CPU_GPIO_33	
129	GSBI5_0 MIC_I2S_MCLK			130	CPU_GPIO_5	
131	PCIE_RX+			132	V5_SB	
133	PCIE_RX-			134	CPU_GPIO_38 CDC_MIC_I2S_DIN1	
135	GSBI5_1 MIC_I2S_WS			136	CPU_GPIO_37 CDC_MIC_I2S_DIN	
137	GPIO_47 I2S2_SCK			138	CPU_GPIO_88	
139	SPKR_I2S_DOUT CPU_GPIO_49			140	RESERVED	
141	GND			142	CPU_GPIO_35 CDC_MIC_I2S_SCK	
143	CPU_GPIO_56			144	CPU_GPIO_36 CDC_MIC_I2S_WS	
145	GPIO_48 I2S2_WS			146	PMIC_MPP_8821_11	
147	SDC2_CMD GPIO_57			148	CPU_GPIO_84	
149	SDC2_DATA_3 GPIO_58			150	V5_SB	
151	SDC2_DATA_2 GPIO_60			152	CPU_GPIO_31 MI2S_SD1	
153	SDC2_DATA_1 GPIO_61			154	PMIC_MPP_8821_10	

Pin #	CM-QS600 Signal Name	Reference Section		Pin #	CM-QS600 Signal Name	Reference Section
155	SDC2_DATA_0 GPIO_62			156	CPU_GPIO_0	
157	SDC2_CLK GPIO_59			158	CPU_USB3_D_N	
159	GND			160	CPU_USB3_D_P	
161	GSBI5_2 MIC_I2S_SCK			162	CPU_GPIO_32 MI2S_SD0	
163	GSBI5_3 MIC_I2S_DIN			164	CPU_USB4_D_N	
165	PWRBTN			166	CPU_USB4_D_P	
167	PMIC_BAT_THERM			168	V5_SB	
169	PMIC_BAT_ID			170	MIPI_DSI0_LN3_P	
171	RSTBTN			172	MIPI_DSI0_LN3_N	
173	MIPI_DSI0_CLK_P			174	USB1_ID	
175	MIPI_DSI0_CLK_N			176	CPU_USB1_D_P	
177	GND			178	CPU_USB1_D_N	
179	PMIC_BMS_CSP			180	V5_OTG	
181	PMIC_BMS_CSN			182	MIPI_DSI0_LN2_P	
183	COIN CELL BATT			184	MIPI_DSI0_LN2_N	
185	CPU_GPIO_50 ALT BOOT I2S2_MCLK			186	V5_SB	
187	CPU_GPIO_1			188	MIPI_DSI0_LN1_P	
189	VREF_BAT			190	MIPI_DSI0_LN1_N	
191	CDC_MIC_BIAS2			192	VBATT	
193	CDC_IN2_P			194	MIPI_DSI0_LN0_P	
195	A_GND			196	MIPI_DSI0_LN0_N	
197	CDC_IN6_P			198	PMIC_MPP_8821_8	
199	CDC_IN5_P			200	PMIC_MPP_8821_9	
201	CDC_HPH_RM			202	PMIC_MPP_8821_7	
203	CDC_HPH_LP			204	V5_SB	

6.2 Mating Connectors

Table 37 Connector type

CM-QS600 connector		Carrier board (mating) connector P/N	
Ref.	Implementation	Mfg.	P/N
P1	2-sides PCB based	Lotes	AAA-DDR-109-K01

6.3 Mechanical Drawings

Figure 2 CM-QS600 Top

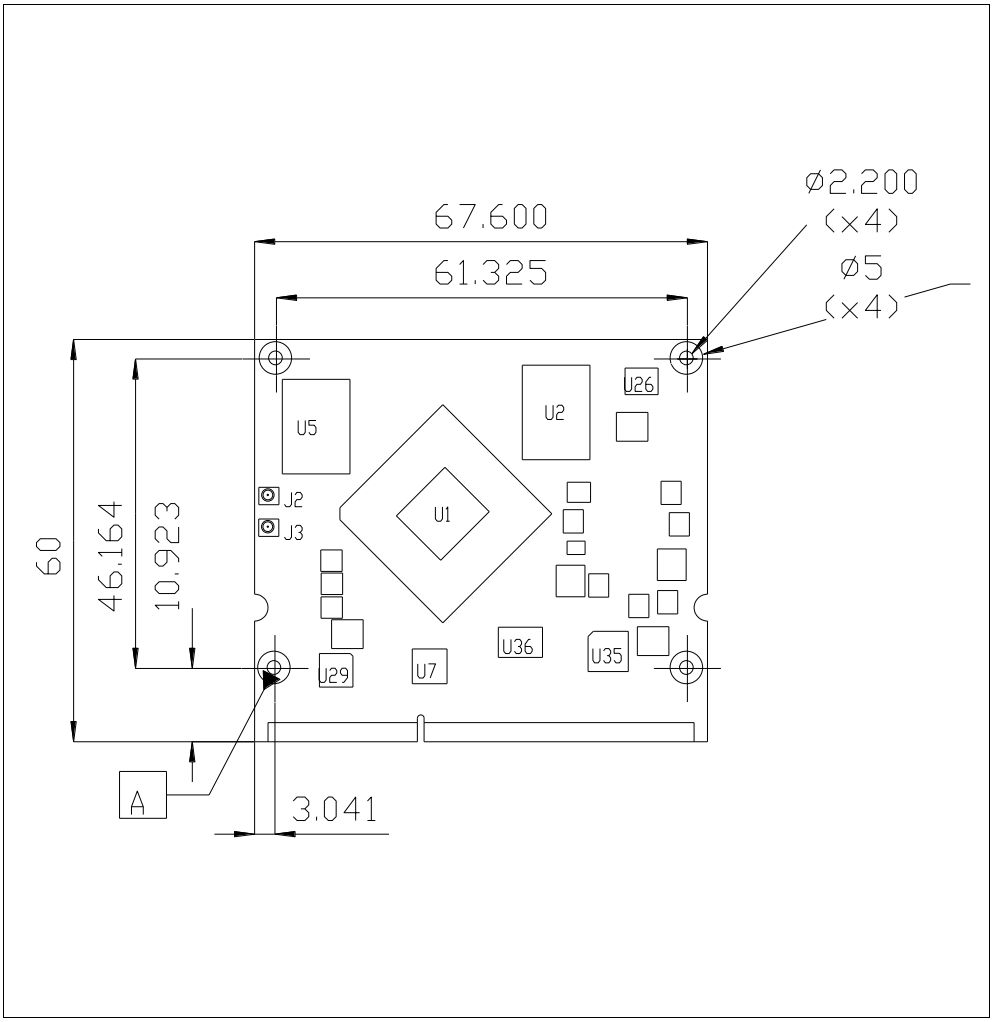
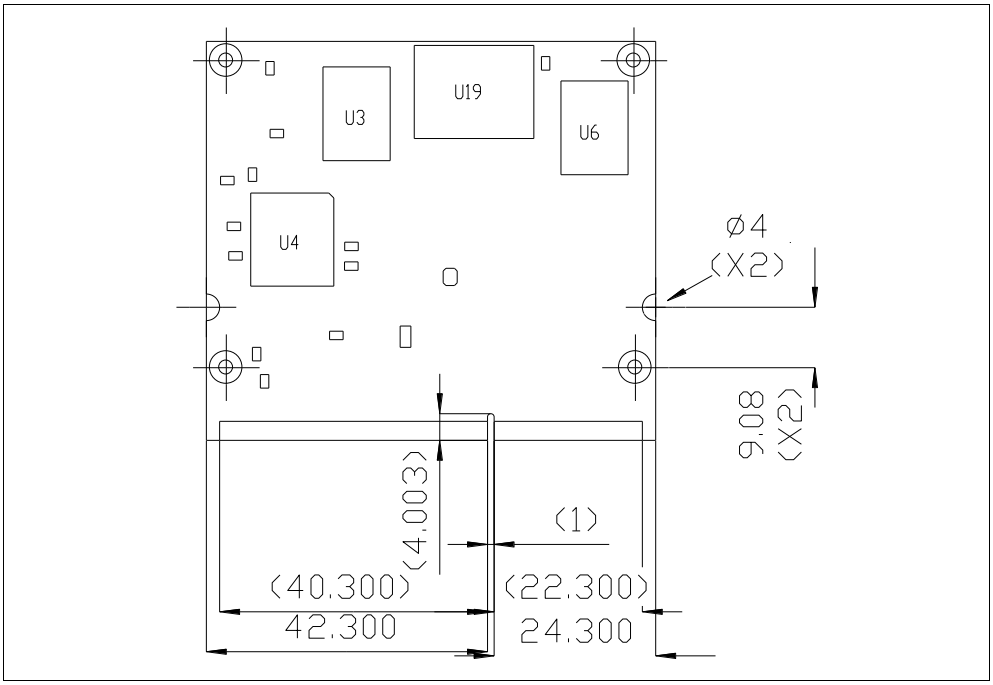


Figure 3 CM-QS600 bottom



1. All dimensions are in millimeters.
2. Height of all components is < 2mm.
3. Baseboard connectors provide 2mm board-to-board clearance.
4. Maximum height of the components which can be placed under the CM-QS600 is 1.0 mm.
5. Board thickness is 1.0mm.

Mechanical drawings are available in DXF format at http://compulab.co.il/products/computer-on-modules/CM-QS600/#devres

6.4 Standoffs/Spacers

CM-QS600 has four mounting holes to physically secure the CoM to the carrier board. Secure CM-QS600 to the carrier board by mounting two spacers with any adequate screws and nuts. Spacers must comply with the following specification:

- M2x0.4 thread, 2.2±0.2 mm length

7 OPERATIONAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

Table 38 Absolute Maximum ratings

Parameter	Limitations	Min	Max	Unit
Main power supply voltage (V5_SB)		-1	6	V
Li-on battery supply voltage (VBATT)		-0.5	6	V
USB OTG VBUS (V5_OTG)		-1	7.5	V
Voltage on any non-power supply pin		-0.5	V_{XX} + 0.5	

NOTE: Exceeding the absolute maximum ratings may damage the device.

NOTE: V_{XX} is the supply voltage associated with the input or output pin to which the test voltage is applied.

7.2 Recommended Operating Conditions

Table 39 Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Main power supply voltage (V5_SB)	4.35	5.0	5.5	V
Backup battery supply voltage (V3_COIN)	2	3.0	3.25	V
Li-on battery supply voltage (VBATT)	2.5	3.6	4.5	
VBUS_5V_OTG		5		V

7.3 DC Electrical Characteristics

Table 40 DC Electrical Characteristics

Parameter	Min	Typ	Max	Unit
Multifunctional Digital I/O				
V_{IH}	1.17		2.1	V
V_{IL}	-0.3		0.63	V
$V_{OH\ (2mA)}$	1.35		1.8	V
$V_{OL\ (2mA)}$	0		0.45	V
SDCARD interface (3.3V)				
V_{IH}	2.3		3.3	V
V_{IL}	-0.3		1.03	V
$V_{OH\ (2mA)}$	2.5		2.95	V
$V_{OL\ (2mA)}$	0		0.45	V

7.4 ESD Performance

Table 41 ESD Performance

Interface	ESD Performance

Multifunctional pins	1kV using Human Body Model (HBM)
USB Host ports (with U4 option)	5kV using Human Body Model (HBM) (differential signals only)

7.5 Operating Temperature Ranges

The CM-QS600 is available with three options of operating temperature range.

Table 42 CM-QS600 Temperature Range Options

Range	Temp.	Description
Commercial	0º to 70º C	Sample boards from each batch are tested for the lower and upper temperature limits. Individual boards are not tested.
Extended	-20º to 70º C	Every board undergoes a short test for the lower limit (-20º C) qualification.
Industrial	-40º to 85º C	Every board is extensively tested for both lower and upper limits and at several midpoints.

8 APPLICATION NOTES

8.1 Carrier Board Design Guidelines

- Ensure that all V5_SB, VBATT, V3_COIN and GND power pins are connected.
- Major power rails – V5_SB and GND must be implemented by planes, rather than traces. Using at least two planes is essential to ensure the system signal quality, because the planes provide a current return path for all interface signals.
- If only regulated power supply is used, insure that PMIC_BMS_CSP and PMIC_BMS_CSN signals connected to GND.
- It is recommended to put several 100nF and 10/100uF capacitors between V5_SB and GND near the mating connectors.
- It is recommended to connect the standoff holes of the carrier board to GND, in order to improve EMC.
- Except for a power connection, no other connection is mandatory for CM-QS600 operation. All power-up circuitry and all required pullups/pulldowns are available onboard CM-QS600.
- If for some reason you decide to place an external pullup or pulldown resistor on a certain signal (for example - on the GPIOs), first check the documentation of that signal provided in this manual. Certain signals have on-board pullup/pulldown resistors required for proper initialization. Overriding their values by external components will disable board operation.
- You must be familiar with signal interconnection design rules. There are many sensitive groups of signals. For example:
  - Ethernet, SATA, USB and more signals must be routed in differential pairs and by a controlled impedance trace.
  - Audio input must be decoupled from possible sources of carrier board noise.
- Be careful when placing components under the CM-QS600 module. The carrier board interface connector provides 1mm mating height. Bear in mind that there are components on the underside of the CM-QS600.
- Refer to the SB-QS600 carrier board reference design schematics.

8.2 Carrier Board Troubleshooting

- Using grease solvent and a soft brush, clean the contacts of the mating connectors of both the module and the carrier board. Remnants of soldering paste can prevent proper contact. Take care to let the connectors and the module dry entirely before re-applying power – otherwise corrosion may occur.
- Using an oscilloscope, check the voltage levels and quality of the V5_SB power supply. Check that there is no excessive ripple or glitches. First perform the measurements without plugging in the module. Then plug in the module and measure again. Measurement should be performed on the pins of the mating connector.
- Using an oscilloscope, verify that the GND pins of the mating connector are indeed at zero voltage level and that there is no ground bouncing. The module must be plugged in during the test.
- Create a "minimum system" - only power, mating connectors, the module, SDCARD interface on SDC-3 and a serial interface.
- Check if the system starts properly. In system larger than the minimum, possible sources of disturbance could be:

- Devices improperly driving the local bus
- External pullup/pulldown resistors overriding the module on-board values, or any other component creating the same "overriding" effect
- Faulty power supply
- In order to avoid possible sources of disturbance, it is strongly recommended to start with a minimal system and then to add/activate off-board devices one by one.
- Check for the existence of soldering shorts between pins of mating connectors. Even if the signals are not used on the carrier board, shorting them on the connectors can disable the module operation. An initial check can be performed using a microscope. However, if microscope inspection finds nothing, it is advisable to check using an X-ray, because often solder bridges are deep beneath the connector body. Note that solder shorts are the most probable factor to prevent a module from booting.
- Check possible signal short circuits due to errors in carrier board PCB design or assembly.
- Improper functioning of a customer carrier board can accidentally delete boot-up code from CM-QS600, or even damage the module hardware permanently. Before every new attempt of activation, check that your module is still functional with CompuLab SB-QS600 carrier board.
- It is recommended to assemble more than one carrier board for prototyping, in order to ease resolution of problems related to specific board assembly.

8.3 Ethernet Magnetics Implementation

8.3.1 Magnetics Selection

Refer to the table below for compatible magnetics. The list of “Qualified Magnetics” contains magnetics verified for proper **functional** operation by CompuLab. Designers should test and qualify all magnetics before using them in an application.

Table 43 Qualified Magnetics

Vendor	P/N	Package
UDE	RTA-1D4B8V1A	Integrated RJ45
PULSE	J1011F01PNL	Integrated RJ45

8.3.2 Magnetics Connection

For magnetic modules connection, please refer to the SB-QS600 reference design schematics

8.4 Heat-plate Integration

To be added in a future revision of this document.