CL-SOM-iMX6UL

Reference Guide

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Table 1 Revision Notes

Date	Description
Dec 2015	First release
Jun 2017	Fixed SODIMM pin-out table 6.1. Fixed GPIO availability table. Updated USB signals tables. Updated PWM, CAN and ADC chapters. Fixed UART tables.

Please check for a newer revision of this manual at the CompuLab website http://www.compulab.com/. Compare the revision notes of the updated manual from the website with those of the printed or electronic version you have.

1 INTRODUCTION

1.1 About This Document

This document is part of a set of reference documents providing information necessary to operate and program CompuLab CL-SOM-iMX6UL Computer-on-Module.

1.2 CL-SOM-iMX6UL Part Number Legend

Please refer to the CompuLab website 'Ordering information' section to decode the CL-SOM-iMX6UL part number: http://www.compulab.com/products/computer-on-modules/cl-som-imx6ul-freescale-imx6-ultralite-system-on-module/#ordering.

1.3 Related Documents

For additional information, refer to the documents listed in Table 2.

Table 2 Related Documents

Document	Location
CL-SOM-iMX6UL Developer Resources	http://www.compulab.com/.../#devres
iMX6UL Reference Manual	http://www.nxp.com/products/...Documentation_Tab
iMX6UL Datasheet	http://www.nxp.com/products/...Documentation_Tab

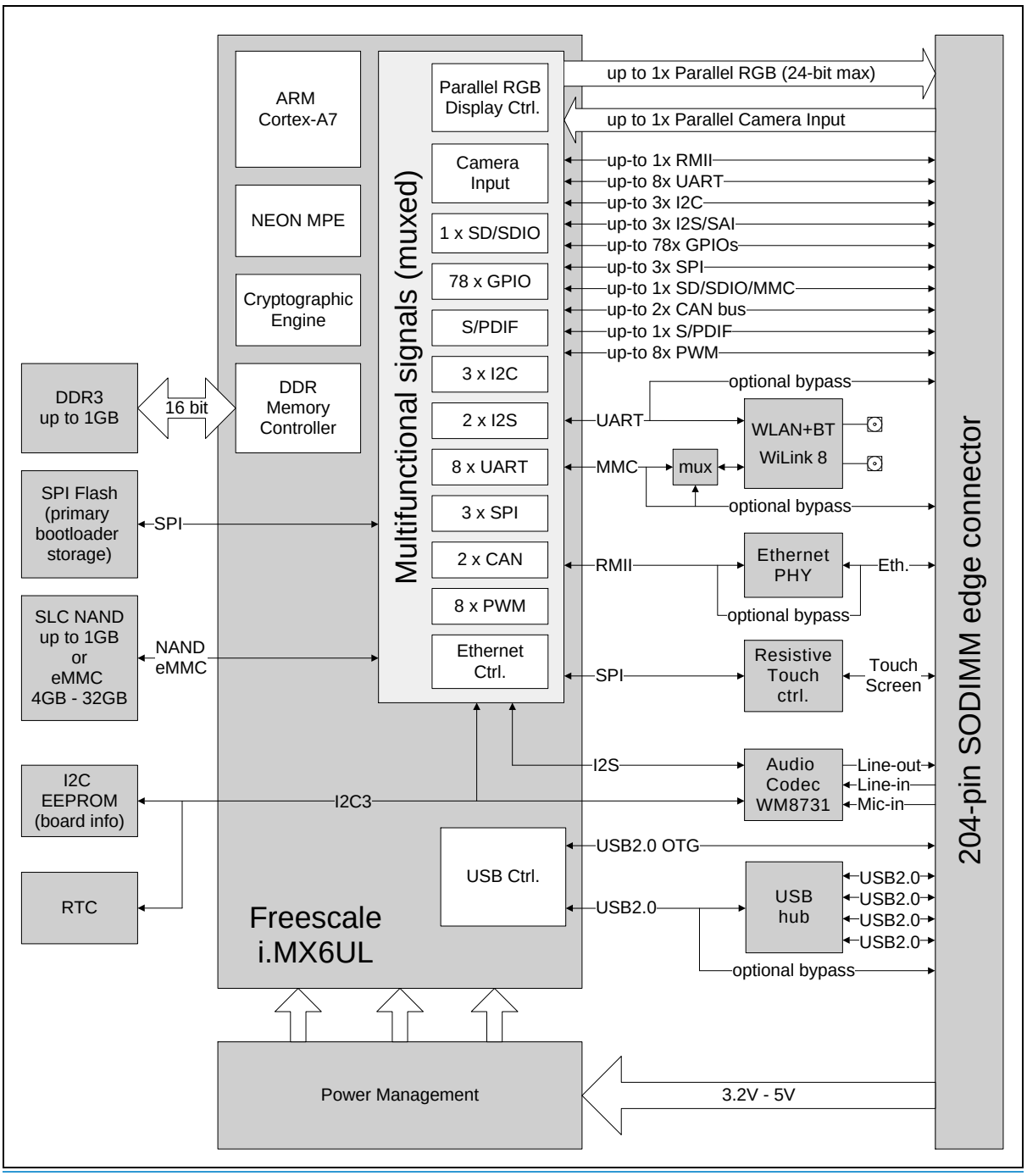
2 OVERVIEW

2.1 Highlights

- NXP i.MX6UL Low Power ARM Cortex-A7 @ 528MHz
- Cortex-A7 NEON MPE (Media Processing Engine) Co-processor
- Up to 1GB Dual Channel DDR3L 16 bit
- Up to 32GB on-board eMMC or raw SLC NAND storage
- LCD Display up to WXGA (1366x768)
- 10/100 Mbit Ethernet, USB2.0 Host/Device (OTG) × 1, USB2.0 Host ×4, UART × 8, SDIO × 2, 12-bit ADC × 2, CAN bus × 2, Touch Screen controller. Onboard WiFi IEEE 802.11a/b/g/n/ac, Onboard Bluetooth 4.0 (supports Low Energy), Onboard Audio CODEC.
- Miniature size: 36 x 68 x 5 mm
- SB-SOM-iMX6UL carrier board turns the CL-SOM-iMX6UL system on module (CoM/SoM) into SBC-iMX6UL, a single board computer

2.2 Block Diagram

Figure 1 CL-SOM-iMX6UL Block Diagram



2.3 CL-SOM-iMX6UL Features

The "Option" column specifies the CoM/SoM configuration option required to have the particular feature. When a CoM/SoM configuration option is prefixed by “NOT”, the particular feature is only available when the option is not used. A feature is only available when a CoM/SoM configuration complies with all options denoted in the “Option” column.
"+" means that the feature is always available.

Table 3 Features and Configuration options

Feature	Description	Option
CPU Core and Graphics		
CPU	NXP i.MX6UL ARM Cortex-A7, 528MHz NEON SIMD and VFPv4	C528
Memory and Storage		
RAM	256MB - 1GB, DDR3-800 with 16-bit bus width.	D
Storage	SLC NAND flash, 128MB - 1GB	N
	eMMC flash, 4GB - 32GB	
Display and Camera		
Display	24-bit parallel display port up to WXGA (1366 x 768) @60Hz	+
Touchscreen	On-board 4-wire resistive touch-screen controller	I
Camera	Parallel camera interface, up to 24-bit	+
Network		
Ethernet	1x 10/100 Mbps Ethernet port (MAC+PHY)	E
	1x RMII 10/100	~~E~~
WiFi	802.11b/g/n WiFi interface, Texas Instruments WiLink 8 WL1801 chipset	W
	Dual-band 2x2 802.11a/b/g/n WiFi interface, Texas Iinstruments WiLink 8 WL1837chipset	WAB
Bluetooth	Bluetooth 4.1 BLE	WAB
Audio		
Analog Audio	WM8731 Audio codec with analog stereo output, stereo input, and electret microphone support	A
	MQS audio interface	+
Digital Audio	2x I2S compliant digital audio interface	+
	1x I2S compliant digital audio interface	~~A~~
	Sony Philips Digital Interconnect Format (SPDIF)	+
I/O		
USB	1x USB2.0 OTG port	+
	Additional 1x USB2.0 host ports	U2
	Additional 4x USB2.0 host ports	U5
Serial Ports (UARTs)	1x UART debug port - TX, RX Only, levels (UART3)	+
	Up to 6x UART ports, up to 4 Mbps	+
	1x UART port - TX, RX, CTS, RTS	~~WAB~~
CAN bus	Up to 2x CAN bus, 3.3V levels	+
MMC/SD/SDIO	Up to 1x MMC/SD/SDIO interface	+
SPI	Up to 3x SPI	+
I2C	Up to 3x I2C	+
PWM	Up to 8x general purpose PWM signals	+
GPIO	Up to 99x GPIO (multifunctional signals shared with other functions)	+
ADC	2x general-purpose ADC channels	+
System Logic		
RTC	Real-time clock, powered by external battery	+

Table 4 Electrical, Mechanical and Environmental Specifications

Electrical Specifications	
Supply Voltage	3.2V to 5V / Li-Ion battery
Digital I/O voltage	3.3V
Active power consumption	0.5 - 3 W, depending on configuration and system load
RTC battery current consumption	666nA@3V
Mechanical Specifications	
Dimensions	36 x 68 x 5 mm
Weight	12 gram
Connectors	204-pin SO-DIMM edge connector
Environmental and Reliability	
MTTF	> 200,000 hours
Operation temperature (case)	Commercial: 0° to 70° C
	Extended: -20° to 70° C
	Industrial: -40° to 85° C. Click for availability note
Storage temperature	-40° to 85° C
Relative humidity	10% to 90% (operation)
	05% to 95% (storage)
Shock	50G / 20 ms
Vibration	20G / 0 - 600 Hz

3 CORE SYSTEM COMPONENTS

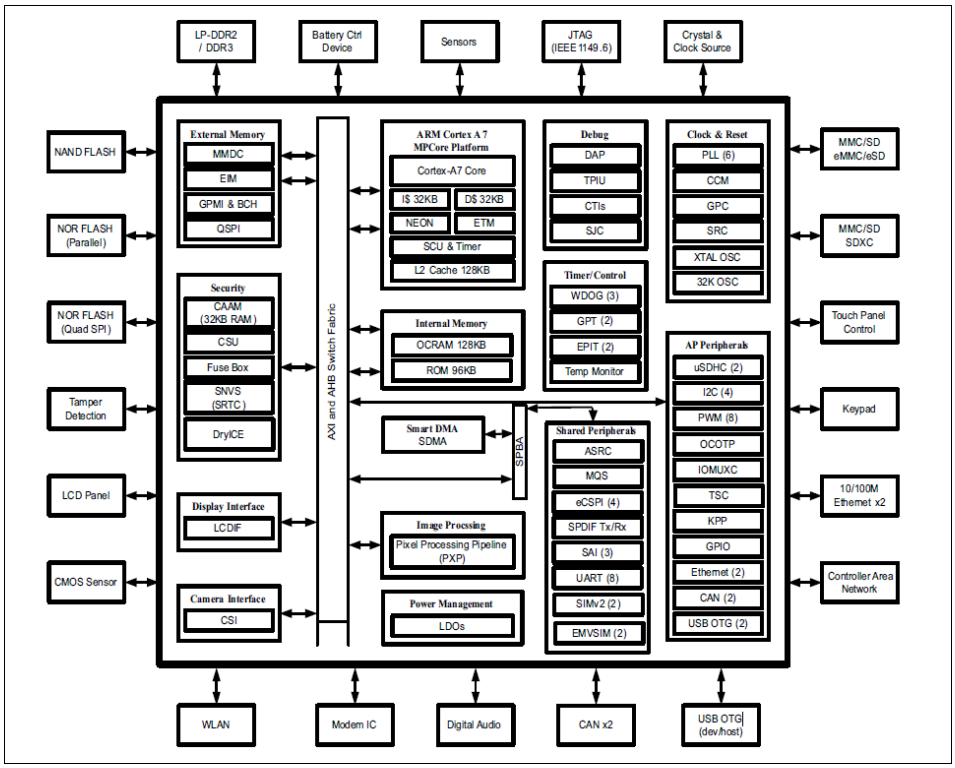
3.1 iMX6UL SoC

The i.MX 6UltraLite is an ultra-efficient processor family with featuring NXP's advanced implementation of the single ARM Cortex®-A7 core, which operates at speeds of up to 528 MHz.

The device is composed of the following major subsystems:

- Single-core ARM Cortex-A7 MPCore™ Platform
  - 32 KBytes L1 Instruction Cache
  - 32 KBytes L1 Data Cache
  - Private Timer and Watchdog
  - TrustZone support
  - Cortex-A7 NEON MPE (Media Processing Engine) Co-processor
- PXP—PiXel Processing Pipeline for imagine resize, rotation, overlay, and CSC. Offloading key pixel processing operations are required to support the LCD display applications.

Figure 2 i.MX6UL Block Diagram



3.2 Memory

3.2.1 DRAM

CL-SOM-iMX6UL is equipped with up to 1GB of onboard DDR3 memory. The DDR3 channel is 16-bits wide and operates at 400 MHz clock frequency (DDR3-800).

3.2.2 Bootloader Storage

The CL-SOM-iMX6UL is assembled with 2MBytes of SPI NOR flash. The SPI NOR flash is the primary non-volatile memory device of CL-SOM-iMX6UL, used for the bootloader and configuration blocks storage.

3.2.3 General Purpose Storage

CL-SOM-iMX6UL is available with secondary onboard storage designed to store the operating system and user data. One of the following onboard non-volatile memory devices can be used as the secondary onboard storage.

- On-board eMMC flash (up to 32GBytes).
- On-board raw SLC NAND Flash (up to 1GBytes).

The secondary storage device is designed to store the operating system (kernel & root filesystem) and general purpose (user) data.

4 PERIPHERAL INTERFACES

CL-SOM-iMX6UL implements a variety of peripheral interfaces through the SODIMM-204 carrier board connector. The following notes apply to interfaces available through the SODIMM-204 interface:

- Some interfaces/signals are available only with/without certain configuration options of the CL-SOM-iMX6UL SoM. The availability restrictions of each signal are described in the "Signals description" table for each interface.
- Some of the CL-SOM-iMX6UL carrier board interface pins are multifunctional. Up to 7 functions (ALT modes) are accessible through each multifunctional pin. Multifunctional pins are denoted with an asterisk (*). For additional details, please refer to chapter 5.6.
- All of the CL-SOM-iMX6UL digital interfaces operate at 3.3V voltage levels unless otherwise noted.

The signals for each interface are described in the "Signal description" table for the interface in question. The following notes provide information on the "Signal description" tables:

- **"Signal name"** – The name of each signal with regards to the discussed interface. The signal name corresponds to the relevant function in cases where the carrier board pin in question is multifunctional.
- **"Pin#" –** The carrier board interface pin number where the discussed signal is available, multifunctional pins are denoted with an asterisk.
- **"Type" –** Signal type, see the definition of different signal types below
- **"Description" –** Signal description with regards to the interface in question.
- **"Availability" –** Depending on CL-SOM-iMX6UL Configuration options, certain carrier board interface pins are physically disconnected (floating) on-board CM-SOM-IMX6UL. The "Availability" column summarizes configuration requirements for each signal. All the listed requirements must be met (logical AND) for a signal to be "available" unless otherwise noted.

Each described signal can be one of the following types. Signal type is noted in the "Signal description" tables. Multifunctional pin direction, pull resistor, and open drain functionality is software controlled. The "Type" column header for multifunctional pins refers to the recommended pin configuration with regards to the discussed signal.

- **"AI"** – Analog Input
- **"AO"** – Analog Output
- **"AIO"** – Analog Input/Output
- **"AP"** – Analog Power Output
- **"I"** – Digital Input
- **"O"** – Digital Output
- **"IO"** – Digital Input/Output
- **"P"** – Power
- **"PD"** - Always pulled down onboard CM-SOM-IMX6UL, followed by pull value.
- **"PU"** - Always pulled up onboard CM-SOM-IMX6UL, followed by pull value.
- **"LVDS"** - Low-voltage differential signaling.

4.1 Parallel Display interface

CL-SOM-iMX6UL Display interface is derived from the i.MX6UL eLCDIF subsystem. The eLCDIF is a general purpose display controller used to drive a broad range of display devices varying in size and capability. The eLCDIF is designed to support dumb (synchronous 24-bit Parallel RGB interface) and smart (asynchronous parallel MPU interface) LCD devices.

For more detailed information, please refer to the i.MX6UL TRM chapter 33: Enhanced LCD Interface (eLCDIF).

The block has several major features:

- Bus master interface to source frame buffer data for display refresh. This interface can also be used to drive data for "Smart" displays.
- PIO interface to manage data transfers between "Smart" displays and SoC.
- 8/16/18/24 bit LCD data bus support available depending on I/O mux options.
- Programmable timing and parameters for MPU, VSYNC and DOTCLK LCD interfaces to support a wide variety of displays.
- ITU-R BT.656 mode (called Digital Video Interface or DVI mode here) including progressive-to-interlace feature and RGB to YCbCr 4:2:2 color space conversion to support 525/60 and 625/50 operation.

The table below summarizes the Parallel Display interface signals

Table 5 Parallel Display Interface Signals

Signal Name	Pin #	Type	Description	Availability
LCD_DATA0	106*	O;PD10K	Data signal	Always available
LCD_DATA1	108*	IO;PD10K	Data signal	Always available
LCD_DATA10	128*	IO;PD10K	Data signal	Always available
LCD_DATA11	130*	IO;PD10K	Data signal	Always available
LCD_DATA12	134*	IO;PD10K	Data signal	Always available
LCD_DATA13	136*	IO;PU10K	Data signal	Always available
LCD_DATA14	138*	IO;PD10K	Data signal	Always available
LCD_DATA15	140*	IO;PD10K	Data signal	Always available
LCD_DATA16	94*	IO;PU10K	Data signal	Always available
LCD_DATA17	92*	IO;PU10K	Data signal	Always available
LCD_DATA18	142*	IO;PD10K	Data signal	Always available
LCD_DATA19	144*	IO;PU10K	Data signal	Always available
LCD_DATA2	110*	IO;PD10K	Data signal	Always available
LCD_DATA20	146*	IO;PD10K	Data signal	Always available
LCD_DATA21	148*	IO;PD10K	Data signal	Always available
LCD_DATA22	74*	IO;PD10K	Data signal	Always available
LCD_DATA23	76*	IO;PD10K	Data signal	Always available
LCD_DATA3	112*	IO;PD10K	Data signal	Always available
LCD_DATA4	116*	IO;PU10K	Data signal	Always available
LCD_DATA5	118*	IO;PU10K	Data signal	Always available
LCD_DATA6	120*	IO;PD10K	Data signal	Always available
LCD_DATA7	122*	IO;PD10K	Data signal	Always available
LCD_DATA8	124*	IO;PD10K	Data signal	Always available
LCD_DATA9	126*	IO;PD10K	Data signal	Always available
LCD_DE	104*	O	Enable signal	Always available
LCD_HSYNC	100*	O	HSYNC signal	Always available
LCD_PCLK	98*	O	Pixel clock signal	Always available
LCD_VSYNC	102*	O	VSYNC signal	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.2 Parallel Camera Interface

The CL-SOM-iMX6UL Camera interface is derived from the i.MX6UL CMOS Sensor Interface (CSI). The CSI enables the chip to connect directly to external CMOS image sensors.

For more detailed information, please refer to the i.MX6UL TRM chapter 19: CMOS Sensor Interface (CSI).

The capabilities of the CSI include:

- Configurable interface logic to support most commonly available CMOS sensors.
- Support for CCIR656 video interface as well as a traditional sensor interface.
- 8-bit / 24-bit data port for YCbCr, YUV, or RGB data input.
- 8-bit / 10-bit / 16-bit data port for Bayer data input.
- Full control of 8-bit/pixel, 10-bit/pixel or 16-bit / pixel data format to 32-bitreceive FIFO packing.

The table below summarizes the Parallel Camera interface signals

Table 6 Parallel Camera Interface Interface Signals

Signal Name	Pin #	Type	Description	Availability
CSI_DATA0	94*	I	Data Sensor Signal	Always available
CSI_DATA0	117*	I	Data Sensor Signal	Always available
CSI_DATA1	111*	I	Data Sensor Signal	Always available
CSI_DATA10	7*	I	Data Sensor Signal	Only w/o ‘WAB’ option.
CSI_DATA10	88*	I	Data Sensor Signal	Always available, SD1_SEL depended with 'W' and 'WAB' options
CSI_DATA11	9*	I	Data Sensor Signal	Always available
CSI_DATA11	144*	I	Data Sensor Signal	Always available
CSI_DATA12	69*	I	Data Sensor Signal	Always available
CSI_DATA12	146*	I	Data Sensor Signal	Always available
CSI_DATA13	58*	I	Data Sensor Signal	Always available
CSI_DATA13	148*	I	Data Sensor Signal	Always available
CSI_DATA14	65*	I	Data Sensor Signal	Always available
CSI_DATA14	74*	I	Data Sensor Signal	Always available
CSI_DATA15	63*	I	Data Sensor Signal	Always available
CSI_DATA15	76*	I	Data Sensor Signal	Always available
CSI_DATA16	12*	I	Data Sensor Signal	Only w/o ‘E’ option.
CSI_DATA16	124*	I	Data Sensor Signal	Always available
CSI_DATA17	14*	I	Data Sensor Signal	Only w/o ‘E’ option.
CSI_DATA17	126*	I	Data Sensor Signal	Always available
CSI_DATA18	109*	I	Data Sensor Signal	Only w/o ‘E’ option.
CSI_DATA18	128*	I	Data Sensor Signal	Always available
CSI_DATA19	6*	I	Data Sensor Signal	Only w/o ‘E’ option.
CSI_DATA19	130*	I	Data Sensor Signal	Always available
CSI_DATA2	101*	I	Data Sensor Signal	Always available
CSI_DATA20	8*	I	Data Sensor Signal	Only w/o ‘E’ option.
CSI_DATA20	134*	I	Data Sensor Signal	Always available
CSI_DATA21	16*	I	Data Sensor Signal	Only w/o ‘E’ option.
CSI_DATA21	136*	I	Data Sensor Signal	Always available
CSI_DATA22	52*	I	Data Sensor Signal	Only w/o ‘E’ option.
CSI_DATA22	138*	I	Data Sensor Signal	Always available
CSI_DATA23	4*	I	Data Sensor Signal	Only w/o ‘E’ option.
CSI_DATA23	140*	I	Data Sensor Signal	Always available
CSI_DATA3	103*	I	Data Sensor Signal	Always available
CSI_DATA4	67*	I	Data Sensor Signal	Always available
CSI_DATA4	89*	I	Data Sensor Signal	Always available
CSI_DATA5	61*	I	Data Sensor Signal	Always available
CSI_DATA5	91*	I	Data Sensor Signal	Always available
CSI_DATA6	11*	I	Data Sensor Signal	Only w/o ‘WAB’ option.
CSI_DATA6	77*	I	Data Sensor Signal	Always available
CSI_DATA7	13*	I	Data Sensor Signal	Only w/o ‘WAB’ option.
CSI_DATA7	79*	I	Data Sensor Signal	Always available
CSI_DATA8	17*	I	Data Sensor Signal	Only w/o ‘WAB’ option.
CSI_DATA8	83*	I	Data Sensor Signal	Always available
CSI_DATA9	15*	I	Data Sensor Signal	Only w/o ‘WAB’ option.
CSI_DATA9	85*	I	Data Sensor Signal	Always available
CSI_FIELD	53*	I	CSI Field Signal	Always available
CSI_HSYNC	115*	I	Horizontal Sync	Always available
CSI_HSYNC	194*	I	Horizontal Sync	Always available
CSI_MCLK	81*	O	CMOS Sensor Master Clock	Only w/o ‘E’ option.

Signal Name	Pin #	Type	Description	Availability
CSI_MCLK	97*	O	CMOS Sensor Master Clock	Always available
CSI_PIXCLK	95*	I	Pixel Clock	Always available
CSI_VSYNC	73*	I	Vertical Sync	Always available
CSI_VSYNC	113*	I	Vertical Sync	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.3 Ethernet

CL-SOM-iMX6UL incorporates a single full-featured 10/100 Ethernet interface, implemented with the i.MX6UL MAC-NET core in conjunction with a 10/100-Mbit/s MAC coupled with an onboard Micrel RMII 10/100 PHY.

4.3.1 100BASE-TX

The CL-SOM-iMX6UL 10/100 MbE interface supports the following main features:

- Integrated PHY for 10/100 Mbps
- IEEE 802.3 Auto-Negotiation support.
- IEEE 802.3ab PHY compliance and compatibility
- Supports automatic MDI/MDIX functions
- Supports 10/100 Mbit/s full duplex and configurable half-duplex operation
- Supports VLAN-tagged frames according to IEEE 802.1Q
- Programmable MAC address: Insertion on transmit; discards frames with mismatching destination address on receive (except broadcast and pause frames)

For CL-SOM-iMX6UL modules w/o “E” options, the i.MX6UL RMII and MDIO lines are routed directly to carrier board interface. Please refer to the iMX6UL Reference manual for additional details.

The table below summarizes the Ethernet 100BASE-TX interface signals

Table 7 Ethernet 100BASE-TX Interface Signals

Signal Name	Pin #	Type	Description	Availability
ENET1_PHY_VDDA	2	P	Center tap supply for Ethernet magnetics.	Only with 'E' option
ENET1_RXN	12	AI	Receive negative input	Only with 'E' option
ENET1_RXP	14	AI	Receive positive input	Only with 'E' option
ENET1_TXN	6	AO	Transmit negative output	Only with 'E' option
ENET1_TXP	8	AO	Transmit positive output	Only with 'E' option
ETH_LED0	16	O;PU10K	Speed indicator LED output. Active (100Mbs) low (pulled up)	Only with 'E' option
ETH_LED1	4	O;PU10K	Activity indicator LED output. Active low (pulled up).	Only with 'E' option

4.3.2 RMII

For CL-SOM-iMX6UL modules w/o “E” options, the i.MX6UL’s Ethernet MAC RMII and MDIO lines are routed directly to carrier board interface. Please refer to the iMX6UL Reference manual for additional details.

The table below summarizes the Ethernet RMII interface signals

Table 8 Ethernet RMII Interface Signals

Signal Name	Pin #	Type	Description	Availability
ENET1_MDC	107*	O	management interface clock	Only w/o 'E' option.
ENET1_MDIO	81*	IO	management interface I/O bidirectional pin	Only w/o 'E' option.
ENET1_RX_EN	109*	I	RMII Carrier Sense/Receive Data Valid	Only w/o 'E' option.
ENET1_RXD0	12*	I	Receive data bit 0 (PHY to MAC)	Only w/o 'E' option.
ENET1_RXD1	14*	I	Receive data bit 1 (PHY to MAC)	Only w/o 'E' option.
ENET1_RXER	4*	IO	Receive Error	Only w/o 'E' option.
ENET1_TXD0	6*	O	Transmit data bit 0 (MAC to PHY)	Only w/o 'E' option.
ENET1_TXD1	8*	O	Transmit data bit 1 (MAC to PHY)	Only w/o 'E' option.

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.4 Wireless Interfaces

CL-SOM-iMX6UL optional wireless communication capabilities are implemented with one of the following two assembly options:

- 2.4GHz WiFi-only capability, Implemented with the "W" ordering option of CL-SOM-iMX6UL. Please refer to WLAN Only section for additional details.
- Dual-Band WiFi and Bluetooth capabilities, Implemented with the "WAB" ordering option of CL-SOM-iMX6UL. Please refer to Dual Band WLAN & Bluetooth section for additional details.

CL-SOM-iMX6UL is equipped with up-to two U.FL high-frequency connectors allowing easy integration with external antennas:

- Primary WLAN/BT antenna connector J1. Can be used with any type of 2.4GHz/5.0GHz antenna for WLAN & Bluetooth functionality. J1 is available with either "W" or "WAB" ordering options of CL-SOM-iMX6UL.
- Secondary WLAN antenna connector J2. Can be used with any type of 2.4GHz/5.0GHz antenna for Dual-Band WLAN functionality. J2 is only available with the "WAB" ordering option of CL-SOM-iMX6UL.

Table 9 J1 & J2 U.FL connector data

Manufacturer	Mfg. P/N	Mating Connector
Hirose	U.FL-R-MT(10)	Hirose U.FL-LP-040

4.4.1 WLAN Only

CL-SOM-iMX6UL simple WLAN Only capabilities are based on the optional Texas Instruments WL1801MOD WLAN module soldered onboard.

WL1801MOD is a WiLink™ 8 based Single-Band combo module enabling Wi-Fi® functionality with CL-SOM-iMX6UL. WL1801MOD supports the following features:

- FCC, IC, ETSI/CE, and TELEC certified with chip antennas.
- Support of IEEE Std 802.11a, 802.11b, 802.11g and 802.11n.
- 20- and 40-MHz SISO and 20-MHz 2 x 2 MIMO at 2.4 GHz for High Throughput: 80 Mbps (TCP), 100 Mbps (UDP).
- 2.4-GHz MRC Support for Extended Range.
- Wi-Fi Direct Concurrent Operation (Multichannel, Multirole).

When populated, WL1801MOD is interfaced with the iMX6UL through the following interfaces:

- iMX6UL MMC/SD/SDIO2 interface is used for WLAN data.

Please refer to the iMX6UL and the Texas Instruments WL1801MOD respective reference manuals for additional details.

NOTE: CL-SOM-iMX6UL WiFi 802.11 b/g/n (without Bluetooth) functionality is available only with the 'W' ordering option.

4.4.2 Dual Band WLAN & Bluetooth

CL-SOM-iMX6UL can be optionally shipped with the Texas Instruments WL1837MOD WLAN/Bluetooh module soldered onboard.

WL1837MOD is a WiLink™ 8 based Dual-Band industrial module enabling Wi-Fi®, Bluetooth®, and Bluetooth Low Energy (BLE) functionality with CL-SOM-iMX6UL. WL1837MOD supports the following features:

- FCC, IC, ETSI/CE, and TELEC certified with chip antennas.
- Support of IEEE Std 802.11a, 802.11b, 802.11g and 802.11n.
- 20- and 40-MHz SISO and 20-MHz 2 x 2 MIMO at 2.4 GHz for High Throughput: 80 Mbps (TCP), 100 Mbps (UDP).
- 2.4-GHz MRC Support for Extended Range and 5-GHz Diversity Capable.
- Wi-Fi Direct Concurrent Operation (Multichannel, Multirole).
- Bluetooth 4.1 Compliance and CSA2 Support.
- Dedicated Audio Processor Support of SBC Encoding + A2DP.
- Dual-Mode Bluetooth and BLE.

When populated, WL1837MOD is interfaced with the iMX6UL through the following interfaces:

- iMX6UL MMC/SD/SDIO2 interface is used for WLAN data.
- iMX6UL UART3 and SAI2 interfaces are employed for Bluetooth and A2DP data.

Please refer to the iMX6UL and the Texas Instruments WL1837MOD respective reference manuals for additional details.

NOTE: CL-SOM-iMX6UL WiFi 802.11 a/b/g/n and Bluetooth functionality is available only with the 'WAB' ordering option.

4.5 Analog Audio

The CL-SOM-iMX6UL analog audio functionality is implemented by interfacing the Wolfson WM8731L audio codec with the iMX6UL SAI2 port. The WM8731L codec supports the following main features:

- Highly Efficient Headphone driver
- Audio performance ('A' weighted): ADC SNR – 90dB, DAC SNR – 100dB.
- Microphone input and electret bias with side tone mixer
- ADC and DAC sampling frequency: 8kHz – 96kHz.
- Selectable ADC high pass filter

NOTE: CL-SOM-iMX6UL Analog audio interface is available only with the 'A' ordering option.

Table 10 Analog Audio Characteristics

Parameter	Test conditions		Min	Typ	Max	Unit
Stereo Headphone Output						
0-dB full-scale output voltage				1.0		Vrms
Maximum output power, PO	Rload = 32Ω			30		mW
	Rload = 16Ω			50		
Signal-to-noise ratio, A-weighted			90	97		dB
Total harmonic distortion	1kHz output, Rload = 32Ω,	Pout = 10mW rms (-5dB)		0.056 -65	0.1 60	% dB
		Pout = 20mW rms (-2dB)		0.56 -45	1.0 40	% dB
Power supply rejection ratio	1 kHz, 100 mVp-p			50		dB
	20Hz – 20kHz, 100mVp-p			45		
Programmable gain	1 kHz output		-73	0	6	dB
Programmable-gain step size	1 kHz			1		dB
Mute attenuation	1 kHz output, 0dB			80		dB
Line Input to ADC						
Input signal level (0 dB)				1.0		Vrms
Signal-to-noise ratio	A-weighted, 0dB gain, Fsample = 48 kHz.		85	90		dB
	A-weighted, 0dB gain, Fsample = 96 kHz.			90		
Dynamic range	A-weighted, −60-dB full-scale input		85	90		dB
Total harmonic distortion	−1-dB input, 0-dB gain			-84 0.006	-74 0.02	dB %
Power supply rejection ratio	1 kHz, 100 mVp-p			50		dB
	20Hz – 20kHz, 100mVp-p			45		
ADC Channel Separation	1 kHz input tone			90		dB
Programmable-gain	1 kHz input tone, Rsource<50Ω		-34.5	0	+12	dB
Programmable-gain step size	Guaranteed Monotonic			1.5		dB
Mute attenuation	0dB, 1 kHz input tone			80		dB
Input resistance	12 dB input gain		10	15		kΩ
	0 dB input gain		20	30		
Input capacitance				10		pF
Microphone Input to ADC						
Input signal level (0 dB)				1.0		Vrms
Signal-to-noise ratio	A-weighted, 0-dB gain			85		dB
Dynamic range,	A-weighted, −60-dB full-scale input			85		dB
Total harmonic distortion,	0dB input, 0dB gain			-60	-55	dB
Power supply rejection ratio	1 kHz, 100 mVp-p			50		dB
	20Hz – 20kHz, 100mVp-p			45		
Programmable-gain Boost	1kHz input, Rsource<50Ω, MICBOOST bit is 1.			34		dB
Mic Path gain (MICBOOST gain is additional to this nominal gain)	MICBOOST bit is 0, Rsource<50Ω,			14		dB
Mute attenuation	0dB, 1 kHz input tone			80		dB
Input resistance				10		kΩ
Input capacitance				10		pF
Microphone Bias						
Bias voltage			2.375	2.475	2.575	V
Bias-current source					3	mA
Output noise voltage	1kHz to 20kHz			25		nV/√Hz

Please refer to the Wolfson Microelectronics WM8731L datasheet for additional details. The table below summarizes the analog audio interface signals

Table 11 Analog Audio Interface Signals

Signal Name	Pin #	Type	Description	Availability
LHPOUT	203	AO	Left channel headphone output	Only with "A" option
LLINEIN	199	AI	Left channel line input	Only with "A" option
MICBIAS	191	AP	Electret microphone bias supply	Only with "A" option
MICIN	193	AI	Microphone input	Only with "A" option

Signal Name	Pin #	Type	Description	Availability
RHPOUT	201	AO	Right channel headphone output	Only with "A" option
RLINEIN	197	AI	Right channel line input	Only with "A" option

4.6 Digital Audio (SAI)

CL-SOM-iMX6UL enables access to all 3 of the iMX6UL integrated synchronous audio interface (SAI) modules. The SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces. The following main features are supported:

- One transmitter with independent bit clock and frame sync supporting 1 data line. One receiver with independent bit clock and frame sync supporting 1 data line.
- Maximum Frame Size of 32 words.
- Word size of between 8-bits and 32-bits. Separate word size configuration for the first word and remaining words in the frame.
- Asynchronous 32 × 32-bit FIFO for each transmit and receive channel

NOTE: CL-SOM-iMX6UL SAI2 interface is available only without the 'A' ordering option.

Please refer to the iMX6UL Reference manual for additional details. The tables below summarize the SAI interface signals

Table 12 SAI 1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SAI1_MCLK	103*	IO	Audio Master Clock	Always available
SAI1_MCLK	106*	IO;PD10K	Audio Master Clock	Always available
SAI1_RX_BCLK	91*	IO	Receive Bit Clock	Always available
SAI1_RX_DATA	83*	I	Receive Data	Always available
SAI1_RX_DATA	112*	I	Receive Data	Always available
SAI1_RX_SYNC	89*	IO	Receive Frame Sync	Always available
SAI1_TX_BCLK	79*	IO	Transmit Bit Clock	Always available
SAI1_TX_BCLK	110*	IO	Transmit Bit Clock	Always available
SAI1_TX_DATA	85*	O	Transmit Data	Always available
SAI1_TX_DATA	116*	O	Transmit Data	Always available
SAI1_TX_SYNC	77*	IO	Transmit Frame Sync	Always available
SAI1_TX_SYNC	108*	IO	Transmit Frame Sync	Always available

Table 13 SAI 2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SAI2_MCLK	133*	IO	Audio Master Clock	Only w/o 'A' option.
SAI2_RX_DATA	143*	I	Receive Data	Only w/o 'A' option.
SAI2_TX_BCLK	137*	IO	Transmit Bit Clock	Only w/o 'A' option.
SAI2_TX_DATA	139*	O	Transmit Data	Only w/o 'A' option.
SAI2_TX_SYNC	145*	IO	Transmit Frame Sync	Only w/o 'A' option.

Table 14 SAI 3 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SAI3_MCLK	98*	IO	Audio Master Clock	Always available
SAI3_MCLK	126*	IO	Audio Master Clock	Always available
SAI3_RX_BCLK	130*	IO	Receive Bit Clock	Always available
SAI3_RX_DATA	102*	I	Receive Data	Always available
SAI3_RX_DATA	138*	I	Receive Data	Always available
SAI3_RX_SYNC	128*	IO	Receive Frame Sync	Always available
SAI3_TX_BCLK	100*	IO	Transmit Bit Clock	Always available
SAI3_TX_BCLK	136*	IO	Transmit Bit Clock	Always available
SAI3_TX_DATA	140*	O	Transmit Data	Always available
SAI3_TX_DATA	154*	O	Transmit Data	Always available
SAI3_TX_SYNC	104*	IO	Transmit Frame Sync	Always available
SAI3_TX_SYNC	134*	IO	Transmit Frame Sync	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.7 Medium Quality Sound module (MQS)

The iMX6UL integrated medium-quality sound module (MQS) is used to generate 2-channel, medium-quality, PWM-like audio, via two standard digital GPIO pins, allowing the user to connect stereo speakers or headphones to a power amplifier without an additional DAC chip. The MQS block accepts valid signals from SAI1 and provides up to 20dB output SNR for signals below 10 kHz. MQS provides only simple audio reproduction. No internal pop, click or distortion artifact reduction methods are provided.

Please refer to the iMX6UL Reference manual for additional details.

The table below summarizes the MQS interface signals

Table 15 MQS Interface Signals

Signal Name	Pin #	Type	Description	Availability
MQS_LEFT	76*	O	Left signal output	Always available
MQS_LEFT	131*	O	Left signal output	Only w/o 'I' option.
MQS_LEFT	137*	O	Left signal output	Only w/o 'A' option.
MQS_RIGHT	74*	O	Right signal output	Always available
MQS_RIGHT	145*	O	Right signal output	Only w/o 'A' option.
MQS_RIGHT	174*	O	Right signal output	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.8 Native USB2.0 ports

The iMX6UL SoC is equipped with two high-speed OTG controller modules and integrated high-speed analog USB PHYs. CL-SOM-iMX6UL enables full access to both ports trough the carrier board interface connector. The second OTG USB port is configured as a HOST only mode. The USB ports support the following main features:

- High speed, full speed and low-speed operation in host mode.
- High speed and full speed operation in peripheral mode.
- Up to 8 bidirectional endpoints.
- CL-SOM-iMX6UL USB port 0 (iMX6UL port 1) supports for OTG signaling, session request protocol (SRP), host negotiation protocol (HNP), and attach detection protocol (ADP). ADP support includes dedicated timer hardware and register interface.
- CL-SOM-iMX6UL USB port 1 (iMX6UL port 2) is configured to operate in host only mode onboard CL-SOM-iMX6UL.
- Supports charger detection with USB_OTG1_CHD_B pin (iMX6UL port 1 only) and register interface (both iMX6UL ports)

NOTE: CL-SOM-iMX6UL USB port 1 (iMX6UL port 2) exposed only with the 'U2' ordering option.

Please refer to the iMX6UL Reference manual for additional details.

The tables below summarize the native USB interface signals

Table 16 native USB HOST Interface Signals

Signal Name	Pin #	Type	Description	Availability
CPU_USB2_D_N	170	AIO	USB host port 2 negative data	Only with 'U2' option
CPU_USB2_D_P	172	AIO	USB host port 2 positive data	Only with 'U2' option

Table 17 native USB OTG Interface Signals

Signal Name	Pin #	Type	Description	Availability
ANATOP.OTG1_ID	65*	AIO	USB OTG ID signal	Always available
ANATOP.OTG1_ID	84*	AIO	USB OTG ID signal	Always available, SD1_SEL depended with 'W' and 'WAB' options
ANATOP.OTG1_ID	174*	AIO	USB OTG ID signal	Always available
USB.OTG1_CHD_B	192	O	Charge detect output	Always available
USB.OTG1_PWR	82*	O	VBUS voltage supply control signal	Always available, SD1_SEL depended with 'W' and 'WAB' options
USB.OTG1_PWR	200	O	VBUS voltage supply control signal	Always available
USB.OTG1_VBUS	180	P	VBUS Power input for LDO_USB	Always available
USB_OTG1_DN	178	AIO	USB2.0 OTG negative data	Always available
USB_OTG1_DP	176	AIO	USB2.0 OTG positive data	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.9 Onboard USB2.0 Hub

CL-SOM-iMX6UL is equipped with an optional onboard USB2.0 hub supporting 4 downstream USB2.0 host ports. The 4 additional ports are implemented through a combination of the iMX6UL on-chip USB high-speed OTG 1 port with the CYPRESS CY7C65632 USB hub. The USB hub supports the following main features:

- Three USB 2.0 High Speed (480Mbps) compatible downstream ports
- Supports either Single-TT or Multi-TT configurations for Full-Speed (12Mbps) and Low-Speed (1.5Mbps) connections

NOTE: CL-SOM-iMX6UL onboard USB hub is available only with the 'U5' ordering option.

Please refer to the CYPRESS CY7C65632 datasheet for additional information. The table below summarizes the USB Hub interface signals

Table 18 USB HUB Interface Signals

Signal Name	Pin #	Type	Description	Availability
HUB_USB1_D_N	170	AIO	USB HUB DS port 1 negative data	Only with 'U5' option
HUB_USB1_D_P	172	AIO	USB HUB DS port 1 positive data	Only with 'U5' option
HUB_USB2_D_N	164	AIO	USB host port 2 negative data	Only with 'U5' option
HUB_USB2_D_P	166	AIO	USB host port 2 positive data	Only with 'U5' option
HUB_USB3_D_N	158	AIO	USB host port 3 negative data	Only with 'U5' option
HUB_USB3_D_P	160	AIO	USB host port 3 positive data	Only with 'U5' option
HUB_USB4_D_N	184	AIO	USB host port 4 negative data	Only with 'U5' option

Signal Name	Pin #	Type	Description	Availability
HUB_USB4_D_P	182	AIO	USB host port 4 positive data	Only with 'U5' option
OC#_PU	162	I,PU10K	Over Current Detection. Active low.	Only with 'U5' option
USB_PWR_EN_B	156	O;PU10K	Power enable control signal for USB_OTG2_VBUS supply. Active low.	Only with 'U5' option

4.10 MMC / SD /SDIO

A one MMC/SD/SDIO port is available through the CL-SOM-iMX6UL carrier board interface. The port is derived from the iMX6UL on-chip MMC/SD/SDIO controller IPs (uSDHC). The uSDHC IP supports the following main features:

- Fully compliant with MMC command/response sets and physical layer as defined in the multimedia card system specification, v5.0/v4.4/v4.41/v4.4/v4.3/v4.2.
- Fully compliant with SD command/response sets and physical layer as defined in the SD memory card specifications, v3.0 including high-capacity SDXC cards up to 2 TB.
- 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max).
- 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 200 MHz in both SDR and DDR modes, including HS400 (8-bit transfer mode is only available on uSDHC port 1).
- Dedicated “card detection” and “write protection” signals and (hardware reset not supported).

NOTE: CL-SOM-iMX6UL MMC/SD/SDIO port is muxed with the WLAN module on ‘W’ and ‘WAB’ ordering options.

Please refer to the iMX6UL Reference manual for additional details.

The table below summarizes the MMC/SD/SDIO interface signals

Table 19 MMC/SD/SDIO Interface Signals

Signal Name	Pin #	Type	Description	Availability
SD1_CD_B	61*	I	Card detection pin	Always available
SD1_CD_B	79*	I	Card detection pin	Always available
SD1_CLK	80*	O	Clock for MMC card	Always available, SD1_SEL depended with 'W' and 'WAB' options
SD1_CMD	82*	IO	Command signal	Always available, SD1_SEL depended with 'W' and 'WAB' options
SD1_DATA_0	84*	IO	Card data bit 0	Always available, SD1_SEL depended with 'W' and 'WAB' options
SD1_DATA_1	86*	IO	Card data bit 1	Always available, SD1_SEL depended with 'W' and 'WAB' options
SD1_DATA_2	88*	IO	Card data bit 2	Always available, SD1_SEL depended with 'W' and 'WAB' options
SD1_DATA_3	90*	IO	Card data bit 3	Always available, SD1_SEL depended with 'W' and 'WAB' options
SD1_SEL	21	I,PU10K	SD1 mux output port select. Tie to GND to route SD1 to P1 connector. PU or leave floated for WLAN operation.	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.11 UART

CL-SOM-iMX6UL enables access to all 8 of the iMX6UL universal asynchronous receiver/transmitter (UART) modules based on the UARTv2 IP. The iMX6UL UARTv2 supports the following features:

- High-speed TIA/EIA-232-F compatible.
- 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none).
- Programmable baud rates up to 4 Mbps.
- 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud.
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s).
- Hardware flow control support for a request to send and clear to send signals.
- RS-485 driver direction control.
- DCE/DTE capability.
- RX_DATA input and TX_DATA output can be inverted respectively in RS-232/RS-485 mode.
- Various asynchronous wake mechanisms with the capability to wake the processor from STOP mode through an on-chip interrupt.

NOTE: The UART2 interface is used onboard CL-SOM-iMX6UL for Bluetooth functionality. Using the UART2 interface signals available through the carrier board interface precludes onboard Bluetooth operation.

Please refer to the iMX6UL Reference manual for additional details.

The tables below summarize the UART interface signals

Table 20 UART 1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART1_CTS	67*	I	UART-1 clear to send.	Always available
UART1_RTS	61*	O	UART-1 request to send.	Always available
UART1_RX	135*	I	UART-1 serial data receive	Always available
UART1_TX	129*	O	UART-1 serial data transmit	Always available

Table 21 UART 2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART2_CTS	17*	I	UART-2 clear to send.	Only w/o 'WAB' option.
UART2_RTS	15*	O	UART-2 request to send.	Only w/o 'WAB' option.
UART2_RX	13*	I	UART-2 serial data receive	Only w/o 'WAB' option.
UART2_TX	11*	O	UART-2 serial data transmit	Only w/o 'WAB' option.

Table 22 UART 3 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART3_CTS	52*	I	UART-3 clear to send.	Always available
UART3_CTS	71	I	UART-3 clear to send.	Always available
UART3_RTS	9*	O	UART-3 request to send	Only w/o 'WAB' option.
UART3_RX	117*	I	UART-3 serial data receive	Always available
UART3_TX	111*	O	UART-3 serial data transmit	Always available

Table 23 UART 4 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART4_CTS	100*	I	UART-4 clear to send.	Always available
UART4_RTS	102*	O	UART-4 request to send	Always available
UART4_RX	104*	I	UART-4 serial data receive	Always available
UART4_TX	98*	O	UART-4 serial data transmit	Always available

Table 24 UART 5 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART5_CTS	91*	I	UART-5 clear to send.	Always available
UART5_CTS	194*	I	UART-5 clear to send.	Always available
UART5_RTS	73*	O	UART-5 request to send.	Always available
UART5_RTS	89*	O	UART-5 request to send.	Always available
UART5_RX	63*	I	UART-5 serial data receive	Always available
UART5_RX	103*	I	UART-5 serial data receive	Always available
UART5_TX	65*	O	UART-5 serial data transmit	Always available
UART5_TX	101*	O	UART-5 serial data transmit	Always available

Table 25 UART 6 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART6_CTS	115*	I	UART-6 clear to send.	Always available
UART6_RTS	113*	O	UART-6 request to send.	Always available
UART6_RX	5*	I	UART-6 serial data receive	Always available
UART6_RX	95*	I	UART-6 serial data receive	Always available
UART6_TX	3*	O	UART-6 serial data transmit	Always available
UART6_TX	97*	O	UART-6 serial data transmit	Always available

Table 26 UART 7 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART7_CTS	120*	I	UART-7 clear to send.	Always available
UART7_RTS	122*	O	UART-7 request to send.	Always available
UART7_RX	92*	I	UART-7 serial data receive	Always available
UART7_TX	94*	O	UART-7 serial data transmit	Always available

Table 27 UART 8 Interface Signals

Signal Name	Pin #	Type	Description	Availability
UART8_CTS	116*	I	UART-8 clear to send.	Always available
UART8_RTS	118*	O	UART-8 request to send.	Always available
UART8_RX	148*	I	UART-8 serial data receive	Always available
UART8_TX	146*	O	UART-8 serial data transmit	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.12 I2C

CL-SOM-iMX6UL is equipped with three I2C bus interfaces. The following general features are supported by all I2C bus interfaces:

- Compliant with Philips I2C specification version 2.1
- Supports standard mode (up to 100K bits/s) and fast mode (up to 400K bits/s)
- Multimaster operation
- Master or Slave operation mode.

Please refer to the iMX6UL Reference manual for additional details.

The tables below summarize the I2C interface signals

Table 28 I2C 1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
I2C1_SCL	69*	O	I2C serial clock line	Always available
I2C1_SCL	95*	O	I2C serial clock line	Always available
I2C1_SCL	129*	O	I2C serial clock line	Always available
I2C1_SDA	58*	IO	I2C serial data line	Always available
I2C1_SDA	97*	IO	I2C serial data line	Always available
I2C1_SDA	135*	IO	I2C serial data line	Always available

Table 29 I2C 2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
I2C2_SCL	65*	O	I2C serial clock line	Always available
I2C2_SCL	115*	O	I2C serial clock line	Always available
I2C2_SCL	174*	O	I2C serial clock line	Always available
I2C2_SDA	63*	IO	I2C serial data line	Always available
I2C2_SDA	113*	IO	I2C serial data line	Always available
I2C2_SDA	131*	IO	I2C serial data line	Only w/o 'I' option.

Table 30 I2C 4 Interface Signals

Signal Name	Pin #	Type	Description	Availability
I2C4_SCL	43*	O	I2C serial clock line	Always available
I2C4_SCL	112*	O	I2C serial clock line	Always available
I2C4_SDA	49*	IO	I2C serial data line	Always available
I2C4_SDA	110*	IO	I2C serial data line	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.13 SPI

Up-to three SPI interfaces are accessible through the CL-SOM-iMX6UL carrier board interface. The SPI interfaces are derived from iMX6UL integrated synchronous serial interface (eCSPI). Each instance of the eCSPI port can operate as either a master or as an SPI slave. The following features are supported:

- Data rate up to 52 Mbit/s.
- Full-duplex synchronous serial interface.
- Master/Slave configurable.
- Up-to four chip select signals to support multiple peripherals.
- Transfer continuation function allows unlimited length data transfers.
- 32-bit wide by 64-entry FIFO for both transmit and receive data.
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable.
- Direct Memory Access (DMA) support.

Please refer to the iMX6UL Reference manual for additional details.

The tables below summarize the SPI interface signals

Table 31 SPI 1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SPI1_CLK	77*	O	SPI-1 Master clock out; slave clock in	Always available
SPI1_CLK	146*	O	SPI-1 Master clock out; slave clock in	Always available
SPI1_CS0_N	79*	O	SPI-1 Chip select 0	Always available
SPI1_CS0_N	148*	O	SPI-1 Chip select 0	Always available
SPI1_CS1_N	118*	O	SPI-1 Chip select 1	Always available

Signal Name	Pin #	Type	Description	Availability
SPI1_CS2_N	120*	O	SPI-1 Chip select 2	Always available
SPI1_CS3_N	122*	O	SPI-1 Chip select 3	Always available
SPI1_MISO	76*	I	SPI-1 Master data out; slave data in	Always available
SPI1_MISO	85*	I	SPI-1 Master data out; slave data in	Always available
SPI1_MOSI	74*	O	SPI-1 Master data in; slave data out	Always available
SPI1_MOSI	86*	O	SPI-1 Master data in; slave data out	Always available, SD1_SEL depended with 'W' and 'WAB' options

Table 32 SPI 2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SPI2_CLK	101*	O	SPI-2 Master clock out; slave clock in	Always available
SPI2_CLK	69	O	SPI-2 Master clock out; slave clock in	Only in revision starting 1.1
SPI2_CS0_N	103*	O	SPI-2 Chip select 0	Always available
SPI2_CS0_N	58	O	SPI-2 Chip select 0	Only in revision starting 1.1
SPI2_CS1_N	100*	O	SPI-2 Chip select 1	Always available
SPI2_CS2_N	102*	O	SPI-2 Chip select 2	Always available
SPI2_CS3_N	154*	O	SPI-2 Chip select 3	Always available
SPI2_MISO	91*	I	SPI-2 Master data out; slave data in	Always available
SPI2_MISO	63	I	SPI-2 Master data out; slave data in	Only in revision starting 1.1
SPI2_MOSI	89*	O	SPI-2 Master data in; slave data out	Always available
SPI2_MOSI	65	O	SPI-2 Master data in; slave data out	Only in revision starting 1.1

Table 33 SPI 3 Interface Signals

Signal Name	Pin #	Type	Description	Availability
SPI3_CLK	13*	O	SPI-3 Master clock out; slave clock in	Only w/o 'WAB' option.
SPI3_CS0_N	11*	O	SPI-3 Chip select 0	Only w/o 'WAB' option.
SPI3_MISO	9*	I	SPI-3 Master data out; slave data in	Only w/o 'WAB' option.
SPI3_MOSI	7*	O	SPI-3 Master data in; slave data out	Only w/o 'WAB' option.

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.14 CAN Bus

CL-SOM-iMX6UL is equipped with two instances of the CAN bus controller. Each interface is implemented with the iMX6UL integrated FlexCAN module. The following features are supported by the DCAN module:

- Supports CAN protocol version 2.0B.
- Programmable bit rate up to 1 Mbps.
- Flexible Mailboxes of eight bytes data length
- 100% backwards compatibility with previous FLEXCAN version

Please refer to the iMX6UL Reference manual for additional details.

The tables below summarize the CAN bus interface signals

Table 34 CAN bus 1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
CAN BUS1.RX	9*	I	FLEXCAN bus receive pin	Always available
CAN BUS1.RX	14*	I	FLEXCAN bus receive pin	Only w/o 'E' option.
CAN BUS1.RX	86*	I	FLEXCAN bus receive pin	Always available, SD1_SEL depended with 'W' and 'WAB' options

Signal Name	Pin #	Type	Description	Availability
CAN BUS1.RX	126*	I	FLEXCAN bus receive pin	Always available
CAN BUS1.TX	7*	O	FLEXCAN bus transmit pin	Only w/o ‘WAB’ option.
CAN BUS1.TX	12*	O	FLEXCAN bus transmit pin	Only w/o ‘E’ option.
CAN BUS1.TX	84*	O	FLEXCAN bus transmit pin	Always available, SD1_SEL depended with 'W' and 'WAB' options
CAN BUS1.TX	124*	O	FLEXCAN bus transmit pin	Always available

Table 35 CAN bus 2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
CAN BUS2.RX	6*	I	FLEXCAN bus receive pin	Only w/o ‘E’ option.
CAN BUS2.RX	15*	I	FLEXCAN bus receive pin	Only w/o ‘WAB’ option.
CAN BUS2.RX	90*	I	FLEXCAN bus receive pin	Always available, SD1_SEL depended with 'W' and 'WAB' options
CAN BUS2.RX	130*	I	FLEXCAN bus receive pin	Always available
CAN BUS2.TX	17*	O	FLEXCAN bus transmit pin	Only w/o ‘WAB’ option.
CAN BUS2.TX	88*	O	FLEXCAN bus transmit pin	Always available, SD1_SEL depended with 'W' and 'WAB' options
CAN BUS2.TX	109*	O	FLEXCAN bus transmit pin	Only w/o ‘E’ option.
CAN BUS2.TX	128*	O	FLEXCAN bus transmit pin	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.15 ADC

CL-SOM-iMX6UL is equipped with two instances of the general purpose ADC controller. Each instance is implemented with the iMX6UL integrated 12-bit general purpose analog to digital converter module (ADC). The iMX6UL ADC module supports the following main features:

- 12-bit word size.
- Support single and continuous conversion.
- Support compare mode and channel auto disable if data match the requirement.
- Support average conversion and flexible 4, 8, 16, 32 number of conversion data.
- Configurable sample time and conversion speed / power. Sample rates up to 1MHz.
- Conversion complete, hardware average complete, compare, DMA, time out the flag and interrupt.
- Automatic compare with an interrupt for less than, greater than, and equal to, within range, or out-of-range, a programmable value.

NOTE: CL-SOM-iMX6UL ADC port 1 is available only without the ‘I’ ordering option.

NOTE: CL-SOM-IMX6UL ADC port 6 and 7 are available only without the ‘E’ ordering option.

Please refer to the iMX6UL Reference manual for additional details.

The tables below summarize the ADC interface signals

Table 36 ADC 1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
ADC1_IN0	174*	AI	Analog channel 1 input 0	Always available
ADC1_IN1	131*	AI	Analog channel 1 input 1	Only w/o 'I' option.
ADC1_IN2	129*	AI	Analog channel 1 input 2	Always available
ADC1_IN3	135*	AI	Analog channel 1 input 3	Always available
ADC1_IN4	200*	AI	Analog channel 1 input 4	Always available
ADC1_IN5	53*	AI	Analog channel 1 input 5	Always available
ADC1_IN6	81*	AI	Analog channel 1 input 6	Only w/o 'E' option.
ADC1_IN7	107*	AI	Analog channel 1 input 7	Only w/o 'E' option.
ADC1_IN8	73*	AI	Analog channel 1 input 8	Always available
ADC1_IN9	194*	AI	Analog channel 1 input 9	Always available

Table 37 ADC 2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
ADC2_IN0	174*	AI	Analog channel 2 input 0	Always available
ADC2_IN1	131*	AI	Analog channel 2 input 1	Only w/o 'I' option.
ADC2_IN2	129*	AI	Analog channel 2 input 2	Always available
ADC2_IN3	135*	AI	Analog channel 2 input 3	Always available
ADC2_IN4	200*	AI	Analog channel 2 input 4	Always available
ADC2_IN5	53*	AI	Analog channel 2 input 5	Always available
ADC2_IN6	81*	AI	Analog channel 2 input 6	Only w/o 'E' option.
ADC2_IN7	107*	AI	Analog channel 2 input 7	Only w/o 'E' option.
ADC2_IN8	73*	AI	Analog channel 2 input 8	Always available
ADC2_IN9	194*	AI	Analog channel 2 input 9	Always available

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.16 Resistive Touch Interface

CL-SOM-iMX6UL features an optional onboard Texas Instruments TSC2046 resistive touch-screen controller. The controller is communicating with the iMX6UL SoC over the SPI4 interface. The interface supports 4-wire touch panels and is available through the CL-SOM-iMX6UL carrier board interface.

NOTE: CL-SOM-iMX6UL Resistive touch interface is available only with the 'I' ordering option.

Please refer to Texas Instruments TSC2046 datasheet for additional details.

The table below summarizes the resistive touch interface signals

Table 38 Resistive Touch Interface Signals

Signal Name	Pin #	Type	Description	Availability
TS_X-	68	AI	Resistive Touch X- (left)	Only with 'I' option.
TS_X+	66	AI	Resistive Touch X+ (right)	Only with 'I' option.
TS_Y-	72	AI	Resistive Touch Y- (bottom)	Only with 'I' option.
TS_Y+	70	AI	Resistive Touch Y+ (top)	Only with 'I' option.

4.17 PWM

Eight PWM output signals are available at the CL-SOM-iMX6UL carrier board interface. The following key features are supported:

- 16-bit up-counter with clock source selection
- 4 x 16 FIFO to minimize interrupt overhead

- 12-bit prescaler for division of clock
- Sound and melody generation
- Active high or active low configured output
- Interrupts at compare and rollover

Please refer to the iMX6UL Reference manual for additional details.

The tables below summarize the PWM interface signals

Table 39 PWM 1 Interface Signals

Signal Name	Pin #	Type	Description	Availability
PWM1.OUT	12*	O	PWM1 functional output	Only w/o 'E' option.
PWM1.OUT	73*	O	PWM1 functional output	Always available
PWM1.OUT	106*	O;PD10K	PWM1 functional output	Always available

Table 40 PWM 2 Interface Signals

Signal Name	Pin #	Type	Description	Availability
PWM2.OUT	14*	O	PWM2 functional output	Only w/o 'E' option.
PWM2.OUT	108*	O	PWM2 functional output	Always available
PWM2.OUT	194*	O	PWM2 functional output	Always available

Table 41 PWM 3 Interface Signals

Signal Name	Pin #	Type	Description	Availability
PWM3.OUT	110*	O	PWM3 functional output	Always available
PWM3.OUT	200*	O	PWM3 functional output	Always available

Table 42 PWM 4 Interface Signals

Signal Name	Pin #	Type	Description	Availability
PWM4.OUT	52*	O	PWM4 functional output	Always available
PWM4.OUT	112*	O	PWM4 functional output	Always available

Table 43 PWM 5 Interface Signals

Signal Name	Pin #	Type	Description	Availability
PWM5.OUT	8*	O	PWM5 functional output	Only w/o 'E' option.
PWM5.OUT	99*	O	PWM5 functional output	Always available
PWM5.OUT	142*	O	PWM5 functional output	Always available

Table 44 PWM 6 Interface Signals

Signal Name	Pin #	Type	Description	Availability
PWM6.OUT	16*	O	PWM6 functional output	Only w/o 'E' option.
PWM6.OUT	99*	O	PWM6 functional output	Always available
PWM6.OUT	137*	O	PWM6 functional output	Only w/o 'A' option.

Table 45 PWM 7 Interface Signals

Signal Name	Pin #	Type	Description	Availability
PWM7.OUT	52*	O	PWM7 functional output	Only w/o 'E' option.
PWM7.OUT	113*	O	PWM7 functional output	Always available
PWM7.OUT	143*	O	PWM7 functional output	Only w/o 'A' option.

Table 46 PWM 8 Interface Signals

Signal Name	Pin #	Type	Description	Availability
PWM8.OUT	4*	O	PWM8 functional output	Only w/o 'E' option.
PWM8.OUT	115*	O	PWM8 functional output	Always available
PWM8.OUT	139*	O	PWM8 functional output	Only w/o 'A' option.

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

4.18 GPIO

Up-to 99 of the iMX6UL general purpose input/output (GPIO) signals are available through the carrier board interface of CL-SOM-iMX6UL. When configured as an output, it is possible to write to an iMX6UL register to control the state driven on the output pin. When configured as an input, it is possible to detect the state of the input by reading the state of an iMX6UL register. In addition, GPIOs peripheral can produce interrupts. The GPIO signals can be configured for the following applications:

NOTE: Not all GPIO signals supported by the iMX6UL SoC are available through the CL-SOM-iMX6UL carrier board interface.

Please refer to the iMX6UL Reference manual for additional details.

The table below summarizes the GPIO interface signals

Table 47 GPIO Interface Signals

Signal Name	Pin #	Type	Description	Availability
GPIO1_00	174*	IO	GPIO	Always available
GPIO1_01	131*	IO	GPIO	Only w/o 'I' option.
GPIO1_02	129*	IO	GPIO	Always available
GPIO1_03	135*	IO	GPIO	Always available
GPIO1_04	200*	IO	GPIO	Always available
GPIO1_05	53*	IO	GPIO	Always available
GPIO1_06	81*	IO	GPIO	Only w/o 'E' option.
GPIO1_07	107*	IO	GPIO	Only w/o 'E' option.
GPIO1_08	73*	IO	GPIO	Always available
GPIO1_09	194*	IO	GPIO	Always available
GPIO1_10	75	IO	GPIO	Always available
GPIO1_11	133*	IO	GPIO	Only w/o 'A' option.
GPIO1_12	145*	IO	GPIO	Only w/o 'A' option.
GPIO1_13	137*	IO	GPIO	Only w/o 'A' option.
GPIO1_14	143*	IO	GPIO	Only w/o 'A' option.
GPIO1_15	139*	IO	GPIO	Only w/o 'A' option.
GPIO1_18	67*	IO	GPIO	Always available
GPIO1_19	61*	IO	GPIO	Always available
GPIO1_20	11*	IO	GPIO	Only w/o 'WAB' option.
GPIO1_21	13*	IO	GPIO	Only w/o 'WAB' option.
GPIO1_22	17*	IO	GPIO	Only w/o 'WAB' option.
GPIO1_23	15*	IO	GPIO	Only w/o 'WAB' option.
GPIO1_24	111*	IO	GPIO	Always available
GPIO1_25	117*	IO	GPIO	Always available
GPIO1_26	7*	IO	GPIO	Only w/o 'WAB' option.
GPIO1_27	9*	IO	GPIO	Only w/o 'WAB' option.
GPIO1_28	69*	IO	GPIO	Always available
GPIO1_29	99*	IO	GPIO	Always available
GPIO1_30	65*	IO	GPIO	Always available
GPIO1_31	63*	IO	GPIO	Always available
GPIO2_00	12*	IO	GPIO	Only w/o 'E' option.
GPIO2_01	14*	IO	GPIO	Only w/o 'E' option.
GPIO2_02	109*	IO	GPIO	Only w/o 'E' option.
GPIO2_03	6*	IO	GPIO	Only w/o 'E' option.
GPIO2_04	8*	IO	GPIO	Only w/o 'E' option.
GPIO2_05	16*	IO	GPIO	Only w/o 'E' option.
GPIO2_06	52*	IO	GPIO	Only w/o 'E' option.
GPIO2_07	4*	IO	GPIO	Only w/o 'E' option.
GPIO2_08	3*	IO	GPIO	Always available
GPIO2_09	5*	IO	GPIO	Always available
GPIO2_10	43*	IO	GPIO	Always available
GPIO2_11	49*	IO	GPIO	Always available

Signal Name	Pin #	Type	Description	Availability
GPIO2_16	82*	IO	GPIO	Always available, SD1_SEL depended with 'W' and 'WAB' options
GPIO2_17	80*	IO	GPIO	Always available, SD1_SEL depended with 'W' and 'WAB' options
GPIO2_18	84*	IO	GPIO	Always available, SD1_SEL depended with 'W' and 'WAB' options
GPIO2_19	86*	IO	GPIO	Always available, SD1_SEL depended with 'W' and 'WAB' options
GPIO2_20	88*	IO	GPIO	Always available, SD1_SEL depended with 'W' and 'WAB' options
GPIO2_21	90*	IO	GPIO	Always available, SD1_SEL depended with 'W' and 'WAB' options
GPIO3_00	98*	IO	GPIO	Always available
GPIO3_01	104*	IO	GPIO	Always available
GPIO3_02	100*	IO	GPIO	Always available
GPIO3_03	102*	IO	GPIO	Always available
GPIO3_04	106*	IO;PD10K	GPIO	Always available
GPIO3_05	108*	IO	GPIO	Always available
GPIO3_06	110*	IO	GPIO	Always available
GPIO3_07	112*	IO	GPIO	Always available
GPIO3_08	114	IO	GPIO	Always available
GPIO3_09	116*	IO	GPIO	Always available
GPIO3_10	118*	IO	GPIO	Always available
GPIO3_11	120*	IO	GPIO	Always available
GPIO3_12	122*	IO	GPIO	Always available
GPIO3_13	124*	IO	GPIO	Always available
GPIO3_14	126*	IO	GPIO	Always available
GPIO3_15	128*	IO	GPIO	Always available
GPIO3_16	130*	IO	GPIO	Always available
GPIO3_17	132	IO	GPIO	Always available
GPIO3_18	134*	IO	GPIO	Always available
GPIO3_19	136*	IO	GPIO	Always available
GPIO3_20	138*	IO	GPIO	Always available
GPIO3_21	94*	IO	GPIO	Always available
GPIO3_22	92*	IO	GPIO	Always available
GPIO3_23	142*	IO	GPIO	Always available
GPIO3_24	144*	IO	GPIO	Always available
GPIO3_25	146*	IO	GPIO	Always available
GPIO3_26	148*	IO	GPIO	Always available
GPIO3_27	74*	IO	GPIO	Always available
GPIO3_28	76*	IO	GPIO	Always available
GPIO4_14	152	IO	GPIO	Always available
GPIO4_16	99*	IO	GPIO	Always available
GPIO4_17	97*	IO	GPIO	Always available
GPIO4_18	95*	IO	GPIO	Always available
GPIO4_19	113*	IO	GPIO	Always available
GPIO4_20	115*	IO	GPIO	Always available
GPIO4_21	101*	IO	GPIO	Always available
GPIO4_22	103*	IO	GPIO	Always available
GPIO4_23	89*	IO	GPIO	Always available
GPIO4_24	91*	IO	GPIO	Always available
GPIO4_25	77*	IO	GPIO	Always available
GPIO4_26	79*	IO	GPIO	Always available
GPIO4_27	83*	IO	GPIO	Always available
GPIO4_28	85*	IO	GPIO	Always available
GPIO5_00	54	IO	GPIO	Only w/o ‘WAB’ option.
GPIO5_01	62	IO	GPIO	Only w/o ‘WAB’ or 'W' option.
GPIO5_02	161	IO	GPIO	Only w/o ‘U5’ option.
GPIO5_03	60	IO	GPIO	Always available
GPIO5_05	56	IO	GPIO	Only w/o ‘E’ option.
GPIO5_06	93	IO	GPIO	Always available
GPIO5_08	59	IO	GPIO	Only w/o ‘E’ option.
GPIO5_09	175	IO	GPIO	Only w/o ‘WAB’ or 'W' option.

NOTE: Pins denoted with "*" are multifunctional. For additional details please refer to chapter 5.5 of this document

5 SYSTEM LOGIC

CL-SOM-iMX6UL allows access to several system logic related signals through the carrier board interface. Please refer to chapter 4 of this document for signal description notes and legend.

5.1 Power Supply

The CL-SOM-iMX6UL supports two power supply options:

- Regulated DC supply (5V Typical).
- Lithium-ion polymer battery
- CL-SOM-iMX6UL does not feature an on-board Lithium-ion polymer battery charger. If required, such a charger must be implemented on the carrier board

Table 48 Power signals

Signal Name	Pin#	Type	Description
VSYS	10,28,46,64,78,96,114 132,150,168,186	P	Main power supply. Connect to a regulated DC supply or Li-iON battery
V3_COIN	183	P	RTC back-up battery power input. Connect to a 3V coin-cell lithium battery. Use 4.7uF capacitor instead of a coin-cell battery if RTC back-up is not required.
ENET1_PHY_VDDA	2	P	Center tap supply for Ethernet magnetics.
USB_OTG1_VBUS	180	P	Supply for USB PHY.
USB_OTG2_VBUS	196	P	Supply for USB PHY. Connect to 5V for H5 version
GND	19,37,55,71,87,105 123,141,159,177,195	P	Common ground.

5.2 System and Miscellaneous Signals

5.2.1 External regulator control and power management

CL-SOM-iMX6UL supports carrier board power supply control by means of two dedicated output signals. Both signals are derived from the iMX6UL SoC. The logic that controls both signals draws its power from the VCC_RTC power rail, meaning that this power supply must always be present in order to use the external regulator control features.

The PMIC_STBY_REQ output can be used to signal carrier board power supply that CL-SOM-iMX6UL is in 'standby' or 'OFF' mode. Utilizing the external regulator control signals enables carrier board power management functionality.

Please refer to the iMX6UL Reference manual for additional details. The table below summarizes the external regulator control signals

Table 49 External regulator control signals

Signal Name	Pin #	Type	Description	Availability
PMIC_STBY_REQ	181	O	When the processor enters SUSPEND mode, it will assert this signal.	Always available
PMIC_ON_REQ	202	O	Active high power-up request output from iMX6UL SoC.	Always available
ONOFF	165	I/PU 100K	Pulled-Up Active low ON/OFF signal (designed for an ONOFF switch). ON and OFF requests can be triggered upon voltage sensed through this signal.	Always available

5.2.2 General Purpose clocks

The iMX6UL clock controller module (CCM) signals are fully accessible through the CL-SOM-iMX6UL carrier board interface.

The CCM allows the iMX6UL SoC to utilize carrier board generated clocks as well as providing on-SoC generated clocks to the carrier board. For additional details, please refer to the "Clock Controller Module (CCM)" of the "i.MX6 Reference Manual".

Table 50 General Purpose clock signals

Signal Name	Pin #	Type	Description	Availability
CCM_CLK1_N	121	LVDS	general purpose differential high speed clock Input/output negative signal	Always
CCM_CLK1_P	119	LVDS	general purpose differential high speed clock Input/output positive signal	Always

5.2.3 Flash Write-protection

The EEPROM_WP signal can be used to prevent accidental corruption of the data stored on the onboard SPI Flash as well as the onboard ID EEPROM. The CL-SOM-iMX6UL on-board EEPROM is used to store board specific production information while the onboard SPI flash is used to store the boot-loader as described in chapter 3.2.2.

NOTE: The EEPROM_WP must be used in conjunction with SW to enable write protection. Using the EEPROM_WP signal alone will not enable write protection.

Table 51 Flash Write protection signals

Signal Name	Pin #	Type	Description	Availability
EEPROM_WP	189	PU	Active low input to enable onboard EEPROM write protection and allow SPI Flash write-protection.	Always available

5.3 Reset

The COLD_RESET_IN signal is the main system reset input. Driving a valid logic zero invokes a global reset that affects every module on CL-SOM-iMX6UL. Please refer to the iMX6UL Reference manual for additional details.

Table 52 Reset signals

Signal Name	Pin #	Type	Description	Availability
COLD_RESET_IN	171	I	Active Low cold reset input signal. Should be used as main system reset A valid pulse is low for at least 31mS, with 5.0nS rise/fall times (max).	Always available

5.4 Boot Sequence

CL-SOM-iMX6UL boot sequence defines which interface/media is used by CL-SOM-iMX6UL to load and execute the initial software (such as U-boot). CL-SOM-iMX6UL can load initial software from the following interfaces/media:

- The on-board primary boot device (SPI Flash with pre-flashed boot-loader).
- An external SD/MMC card using the MMC/SD/SDIO 1 interface

CL-SOM-iMX6UL will query boot devices/interfaces for initial software in the order defined by the active boot sequence. A total of two different boot sequences are supported by CL-SOM-iMX6UL:

- Standard sequence: Designed for normal system operation with the on-board primary boot device as the boot media.
- Alternate sequence: Designed allow recovery from an external boot device in case of data corruption on the on-board primary boot device. Using the alternate sequence allows CL-SOM-iMX6UL to boot from an external SD card, effectively bypassing the onboard SPI Flash.

The initial logic value of ALT_BOOT signal defines which of the supported boot sequences is used by the system.

Table 53 Alternative Boot selection signal

Signal Name	Pin #	Type	Description	Availability
ALT_BOOT	185	I	Active high alternate boot sequence select input. Leave floating or tie low for standard boot sequence	Always available

Table 54 CL-SOM-iMX6UL Boot sequences

sequence	ALT_BOOT	First
Standard	Low or floating	Onboard SPI Flash (Primary boot storage)
Alternate	High	SD card on MMC/SD/SDIO1 interface

5.5 Signal Multiplexing Characteristics

Up to 99 of the CL-SOM-iMX6UL carrier board interface pins are multifunctional. Multifunctional pins enable extensive functional flexibility of the CL-SOM-iMX6UL CoM/SoM by allowing usage of a single carrier board interface pin for one of several functions. Up-to 9 functions (MUX modes) are accessible through each multifunctional carrier board interface pin. The multifunctional capabilities of CL-SOM-iMX6UL pins are derived from the iMX6UL SoC control module

NOTE: Pin function selection is controlled by software.

NOTE: Each pin can be used for a single function at a time.

NOTE: Only one pin can be used for each function (in case a function is available on more than one carrier board interface pin).

NOTE: An empty MUX mode is a "RESERVED" function and must not be used.

Table 55 Multifunctional Signals

Pin #	i.MX6UL signal/ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT8	Availability
3	ENET2_RXD0	UART6.TX		I2C3.SCL		GPIO2.IO[8]			ALWAYS AVAILABLE
4	ENET1_RXER	UART7.RTS_B	PWM8.OUT	CSI.DATA[23]		GPIO2.IO[7]			W/O "E" OPTION
5	ENET2_RXD1	UART6.RX		I2C3.SDA		GPIO2.IO[9]		USB.OTG1_OC	ALWAYS AVAILABLE
6	ENET1_TXD0	UART5.CTS_B		CSI.DATA[19]	CAN2.RX	GPIO2.IO[3]			W/O "E" OPTION
7	UART3_CTS		CAN1.TX	CSI.DATA[10]		GPIO1.IO[26]			ALWAYS AVAILABLE
8	ENET1_TXD1	UART6.CTS_B	PWM5.OUT	CSI.DATA[20]		GPIO2.IO[4]			W/O "E" OPTION
9	UART3_RTS		CAN1.RX	CSI.DATA[11]		GPIO1.IO[27]			ALWAYS AVAILABLE
11	UART2_TXD		I2C4.SCL	CSI.DATA[6]		GPIO1.IO[20]		ECSPI3.SS0	W/O "WAB" OPTION
12	ENET1_RXD0	UART4.RTS_B	PWM1.OUT	CSI.DATA[16]	CAN1.TX	GPIO2.IO[0]			W/O "E" OPTION
13	UART2_RXD		I2C4.SDA	CSI.DATA[7]		GPIO1.IO[21]		ECSPI3.SCLK	W/O "WAB" OPTION
14	ENET1_RXD1	UART4.CTS_B	PWM2.OUT	CSI.DATA[17]	CAN1.RX	GPIO2.IO[1]			W/O "E" OPTION
15	UART2_RTS		CAN2.RX	CSI.DATA[9]		GPIO1.IO[23]		ECSPI3.MISO	W/O "WAB" OPTION
16	ENET1_TXEN	UART6.RTS_B	PWM6.OUT	CSI.DATA[21]		GPIO2.IO[5]			W/O "E" OPTION
17	UART2_CTS		CAN2.TX	CSI.DATA[8]		GPIO1.IO[22]		ECSPI3.MOSI	W/O "WAB" OPTION
43	ENET2_CRS_DV	UART7.TX	SIM1.PORT0_RST_B	I2C4.SCL		GPIO2.IO[10]			ALWAYS AVAILABLE
49	ENET2_TXD0	UART7.RX		I2C4.SDA		GPIO2.IO[11]			ALWAYS AVAILABLE
52	ENET1_TXCLK	UART7.CTS_B	PWM7.OUT	CSI.DATA[22]		GPIO2.IO[6]			W/O "E" OPTION

Pin #	i.MX6UL signal/ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT8	Availability
53	GPIO1_IO05	PWM4.OUT	ANATOP.OTG2_ID	CSI.FIELD		GPIO1.IO[5]		UART5.RX	ALWAYS AVAILABLE
54	SNVS_TAMPER0					GPIO5.IO[0]			W/O “WAB” OPTION
56	SNVS_TAMPER5					GPIO5.IO[5]			W/O “E” OPTION
58	UART4_RXD		I2C1.SDA	CSI.DATA[13]		GPIO1.IO[29]		ECSPI2.SS0	W/O “I” OPTION
59	SNVS_TAMPER8					GPIO5.IO[8]			W/O “E” OPTION
60	SNVS_TAMPER3					GPIO5.IO[3]			ALWAYS AVAILABLE
61	UART1_RTS		USDHC1.CD_B	CSI.DATA[5]		GPIO1.IO[19]			ALWAYS AVAILABLE
62	SNVS_TAMPER1					GPIO5.IO[1]			W/O “W”/“WAB” OPTION
63	UART5_RXD		I2C2.SDA	CSI.DATA[15]		GPIO1.IO[31]		ECSPI2.MISO	ALWAYS AVAILABLE
65	UART5_TXD		I2C2.SCL	CSI.DATA[14]		GPIO1.IO[30]		ECSPI2.MOSI	ALWAYS AVAILABLE
67	UART1_CTS		USDHC1.WP	CSI.DATA[4]		GPIO1.IO[18]			ALWAYS AVAILABLE
69	UART4_TXD		I2C1.SCL	CSI.DATA[12]		GPIO1.IO[28]		ECSPI2.SCLK	ALWAYS AVAILABLE
73	GPIO1_IO08		SPDIF.OUT	CSI.VSYNC		GPIO1.IO[8]		UART5.RTS_B	ALWAYS AVAILABLE
74	LCD_DATA22		ECSPI1.MOSI	CSI.DATA[14]		GPIO3.IO[27]			ALWAYS AVAILABLE
75	JTAG_MOD		SPDIF.OUT			GPIO1.IO[10]			ALWAYS AVAILABLE
76	LCD_DATA23		ECSPI1.MISO	CSI.DATA[15]		GPIO3.IO[28]			ALWAYS AVAILABLE
77	CSI_DATA04		SIM2.PORT1_CLK	ECSPI1.SCLK		GPIO4.IO[25]	SAI1.TX_SYNC	USDHC1.WP	ALWAYS AVAILABLE
79	CSI_DATA05		SIM2.PORT1_RST_B	ECSPI1.SS0		GPIO4.IO[26]	SAI1.TX_BCLK	USDHC1.CD_B	ALWAYS AVAILABLE
80	SD1_CLK		SAI2.MCLK	SPDIF.IN		GPIO2.IO[17]		USB.OTG1_OC	W/O “W”/”WAB” OPTIONS
81	GPIO1_IO06			CSI.MCLK		GPIO1.IO[6]		UART1.CTS_B	W/O “E” OPTION
82	SD1_CMD		SAI2.RX_SYNC	SPDIF.OUT		GPIO2.IO[16]		USB.OTG1_PWR	W/O “W”/”WAB” OPTIONS
83	CSI_DATA06		SIM2.PORT1_SVEN	ECSPI1.MOSI		GPIO4.IO[27]	SAI1.RX_DATA	USDHC1.RESET_B	ALWAYS AVAILABLE
84	SD1_DATA0		SAI2.TX_SYNC	CAN1.TX		GPIO2.IO[18]		ANATOP.OTG1_ID	W/O “W”/”WAB” OPTIONS
85	CSI_DATA07		SIM2.PORT1_TRXD	ECSPI1.MISO		GPIO4.IO[28]	SAI1.TX_DATA		ALWAYS AVAILABLE
86	SD1_DATA1		SAI2.TX_BCLK	CAN1.RX		GPIO2.IO[19]		USB.OTG2_PWR	W/O “W”/”WAB” OPTIONS
88	SD1_DATA2		SAI2.RX_DATA	CAN2.TX		GPIO2.IO[20]		USB.OTG2_OC	W/O “W”/”WAB” OPTIONS
89	CSI_DATA02		SIM1.PORT1_TRXD	ECSPI2.MOSI		GPIO4.IO[23]	SAI1.RX_SYNC	UART5.RTS_B	ALWAYS AVAILABLE
90	SD1_DATA3		SAI2.TX_DATA	CAN2.RX		GPIO2.IO[21]		ANATOP.OTG2_ID	W/O “W”/”WAB” OPTIONS
91	CSI_DATA03		SIM2.PORT1_PD	ECSPI2.MISO		GPIO4.IO[24]	SAI1.RX_BCLK	UART5.CTS_B	ALWAYS AVAILABLE
92	LCD_DATA17	UART7.RX		CSI.DATA[0]		GPIO3.IO[22]			ALWAYS AVAILABLE

Pin #	i.MX6UL signal/ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT8	Availability
93	SNVS_TAMPER6					GPIO5.IO[6]			ALWAYS AVAILABLE
94	LCD_DATA16	UART7.TX		CSI.DATA[1]		GPIO3.IO[21]			ALWAYS AVAILABLE
95	CSI_PIXCLK			I2C1.SCL		GPIO4.IO[18]		UART6.RX	ALWAYS AVAILABLE
97	CSI_MCLK		RAWNAND.CE2_B	I2C1.SDA		GPIO4.IO[17]		UART6.TX	ALWAYS AVAILABLE
98	LCD_CLK		UART4.TX	SAI3.MCLK		GPIO3.IO[0]			ALWAYS AVAILABLE
99	NAND_DQS	CSI.FIELD		PWM5.OUT		GPIO4.IO[16]		SPDIF.EXT_CLK	ALWAYS AVAILABLE
100	LCD_HSYNC		UART4.CTS_B	SAI3.TX_BCLK		GPIO3.IO[2]		ECSPI2.SS1	ALWAYS AVAILABLE
101	CSI_DATA00		SIM1.PORT1_RST_B	ECSPI2.SCLK		GPIO4.IO[21]		UART5.TX	ALWAYS AVAILABLE
102	LCD_VSYNC		UART4.RTS_B	SAI3.RX_DATA		GPIO3.IO[3]		ECSPI2.SS2	ALWAYS AVAILABLE
103	CSI_DATA01		SIM1.PORT1_SVEN	ECSPI2.SS0		GPIO4.IO[22]	SAI1.MCLK	UART5.RX	ALWAYS AVAILABLE
104	LCD_ENABLE		UART4.RX	SAI3.TX_SYNC		GPIO3.IO[1]			ALWAYS AVAILABLE
106	LCD_DATA00	PWM1.OUT			I2C3.SDA	GPIO3.IO[5]		SAI1.MCLK	ALWAYS AVAILABLE
107	GPIO1_IO07			CSI.PIXCLK		GPIO1.IO[7]		UART1.RTS_B	W/O “E” OPTION
108	LCD_DATA01	PWM2.OUT			I2C3.SCL	GPIO3.IO[6]		SAI1.TX_SYNC	ALWAYS AVAILABLE
109	ENET1_CRS_DV	UART5.RTS_B	OSC32K.32K_OUT	CSI.DATA[18]	CAN2.TX	GPIO2.IO[2]			W/O “E” OPTION
110	LCD_DATA02	PWM3.OUT			I2C4.SDA	GPIO3.IO[7]		SAI1.TX_BCLK	ALWAYS AVAILABLE
111	UART3_TXD			CSI.DATA[1]	UART2.CTS_B	GPIO1.IO[24]		ANATOP.OTG1_ID	ALWAYS AVAILABLE
112	LCD_DATA03	PWM4.OUT			I2C4.SCL	GPIO3.IO[8]		SAI1.RX_DATA	ALWAYS AVAILABLE
113	CSI_VSYNC			I2C2.SDA		GPIO4.IO[19]	PWM7.OUT	UART6.RTS_B	ALWAYS AVAILABLE
115	CSI_HSYNC			I2C2.SCL		GPIO4.IO[20]	PWM8.OUT	UART6.CTS_B	ALWAYS AVAILABLE
116	LCD_DATA04	UART8.CTS_B			SPDIF.SR_CLK	GPIO3.IO[9]		SAI1.TX_DATA	ALWAYS AVAILABLE
117	UART3_RXD			CSI.DATA[0]	UART2.RTS_B	GPIO1.IO[25]			ALWAYS AVAILABLE
118	LCD_DATA05	UART8.RTS_B			SPDIF.OUT	GPIO3.IO[10]		ECSPI1.SS1	ALWAYS AVAILABLE
120	LCD_DATA06	UART7.CTS_B			SPDIF.LOCK	GPIO3.IO[11]		ECSPI1.SS2	ALWAYS AVAILABLE
122	LCD_DATA07	UART7.RTS_B			SPDIF.EXT_CLK	GPIO3.IO[12]		ECSPI1.SS3	ALWAYS AVAILABLE
124	LCD_DATA08	SPDIF.IN		CSI.DATA[16]		GPIO3.IO[13]		CAN1.TX	ALWAYS AVAILABLE
126	LCD_DATA09	SAI3.MCLK		CSI.DATA[17]		GPIO3.IO[14]		CAN1.RX	ALWAYS AVAILABLE
128	LCD_DATA10	SAI3.RX_SYNC		CSI.DATA[18]		GPIO3.IO[15]		CAN2.TX	ALWAYS AVAILABLE
129	GPIO1_IO02		USB.OTG2_PWR		USDHC1.WP	GPIO1.IO[2]		UART1.TX	ALWAYS AVAILABLE
130	LCD_DATA11	SAI3.RX_BCLK		CSI.DATA[19]		GPIO3.IO[16]		CAN2.RX	ALWAYS AVAILABLE
131	GPIO1_IO01		USB.OTG1_OC		MQS.LEFT	GPIO1.IO[1]			W/O “I” OPTION

Pin #	i.MX6UL signal/ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT8	Availability
133	JTAG_TMS		SAI2.MCLK			GPIO1.IO[11]			W/O “A” OPTIONS
134	LCD_DATA12	SAI3.TX_SYNC		CSI.DATA[20]		GPIO3.IO[17]			ALWAYS AVAILABLE
135	GPIO1_IO03		USB.OTG2_OC	OSC32K.32K_OUT	USDHC1.CD_B	GPIO1.IO[3]		UART1.RX	ALWAYS AVAILABLE
136	LCD_DATA13	SAI3.TX_BCLK		CSI.DATA[21]		GPIO3.IO[18]			ALWAYS AVAILABLE
137	JTAG_TDI		SAI2.TX_BCLK		PWM6.OUT	GPIO1.IO[13]	MQS.LEFT		W/O “A” OPTIONS
138	LCD_DATA14	SAI3.RX_DATA		CSI.DATA[22]		GPIO3.IO[19]			ALWAYS AVAILABLE
139	JTAG_TRST_B		SAI2.TX_DATA		PWM8.OUT	GPIO1.IO[15]	ANATOP.24M_OUT		W/O “A” OPTIONS
140	LCD_DATA15	SAI3.TX_DATA		CSI.DATA[23]		GPIO3.IO[20]			ALWAYS AVAILABLE
142	LCD_DATA18	PWM5.OUT		CSI.DATA[10]		GPIO3.IO[23]			ALWAYS AVAILABLE
143	JTAG_TCK		SAI2.RX_DATA		PWM7.OUT	GPIO1.IO[14]	OSC32K.32K_OUT		W/O “A” OPTIONS
144	LCD_DATA19	PWM6.OUT	GLOBAL WDOG	CSI.DATA[11]		GPIO3.IO[24]			ALWAYS AVAILABLE
145	JTAG_TDO		SAI2.TX_SYNC			GPIO1.IO[12]	MQS.RIGHT		W/O “A” OPTIONS
146	LCD_DATA20	UART8.TX	ECSPI1.SCLK	CSI.DATA[12]		GPIO3.IO[25]			ALWAYS AVAILABLE
148	LCD_DATA21	UART8.RX	ECSPI1.SS0	CSI.DATA[13]		GPIO3.IO[26]			ALWAYS AVAILABLE
152	NAND_CE1_B	USDHC1.DATA6		ECSPI3.MOSI		GPIO4.IO[14]		UART3.CTS_B	ALWAYS AVAILABLE
154	LCD_RESET			SAI3.TX_DATA		GPIO3.IO[4]		ECSPI2.SS3	ALWAYS AVAILABLE
161	SNVS_TAMPER2					GPIO5.IO[2]			W/O “E” OPTION
174	GPIO1_IO00		ANATOP.OTG1_ID	ANATOP.ENET_REF_CLK1	MQS.RIGHT	GPIO1.IO[0]			ALWAYS AVAILABLE
175	SNVS_TAMPER9					GPIO5.IO[9]			W/O “W”/”WAB” OPTION
194	GPIO1_IO09		SPDIF.IN	CSI.HSYNC		GPIO1.IO[9]	USDHC1.RESET_B	UART5.CTS_B	ALWAYS AVAILABLE
200	GPIO1_IO04	PWM3.OUT	USB.OTG1_PWR	ANATOP.24M_OUT	USDHC1.RESET_B	GPIO1.IO[4]		UART5.TX	ALWAYS AVAILABLE

5.6 RTC

CL-SOM-iMX6UL features an on-board ultra-low-power EM3027 real time clock (RTC). The RTC connected to the i.MX6UL SoC using I2C3 interface at address 56h.

At main power supply absence, in order to maintain activities of the RTC, i.e. clock advancement and data storage, use of a backup power supply is essential. The backup power supply may be derived from a super-cap or a battery. A rechargeable battery can be charged from the VSYS voltage using an internal trickle charger of the RTC.

For more information about RTC refer to the EM3027 datasheet.

5.7 LED

The CL-SOM-iMX6UL features a single general purpose green LED controlled by GPIO5_044 signal of the iMX6UL. The LED is ON when GPIO5_04 is logic High.

6 CARRIER BOARD INTERFACE

The CL-SOM-iMX6UL CoM/SoM carrier board interface uses the SODIMM-204 edge connector. The SoM pinout is detailed in the table below.

6.1 Connector Pinout

Table 56 Connector P1

Pin #	CL-SOM-iMX6UL Signal Name	Ref.	Pin #	CL-SOM-iMX6UL Signal Name	Ref.
1	GND	5.1	2	ENET1_PHY_VDDA	4.3.1
3	UART6_TX GPIO2_08	4.11 4.18	4	CSI_DATA23 ETH_LED1 ENET1_RXER PWM8.OUT GPIO2_07	4.2 4.3.1 4.3.2 4.17 4.18
5	UART6_RX GPIO2_09	4.11 4.18	6	CSI_DATA19 ENET1_TXN ENET1_TXD0 CAN BUS2.RX GPIO2_03	4.2 4.3.1 4.3.2 4.14 4.18
7	CSI_DATA10 SPI3_MOSI CAN BUS1.TX GPIO1_26	4.2 4.13 4.14 4.18	8	CSI_DATA20 ENET1_TXP ENET1_TXD1 PWM5.OUT GPIO2_04	4.2 4.3.1 4.3.2 4.17 4.18
9	CSI_DATA11 UART3_RTS SPI3_MISO CAN BUS1.RX GPIO1_27	4.2 4.11 4.13 4.14 4.18	10	VSYS	5.1
11	CSI_DATA6 UART2_TX SPI3_CS0_N GPIO1_20	4.2 4.11 4.13 4.18	12	CSI_DATA16 ENET1_RXN ENET1_RXD0 CAN BUS1.TX PWM1.OUT GPIO2_00	4.2 4.3.1 4.3.2 4.14 4.17 4.18
13	CSI_DATA7 UART2_RX SPI3_CLK GPIO1_21	4.2 4.11 4.13 4.18	14	CSI_DATA17 ENET1_RXP ENET1_RXD1 CAN BUS1.RX PWM2.OUT GPIO2_01	4.2 4.3.1 4.3.2 4.14 4.17 4.18
15	CSI_DATA9 UART2_RTS CAN BUS2.RX GPIO1_23	4.2 4.11 4.14 4.18	16	CSI_DATA21 ETH_LED0 PWM6.OUT GPIO2_05	4.2 4.3.1 4.17 4.18
17	CSI_DATA8 UART2_CTS CAN BUS2.TX GPIO1_22	4.2 4.11 4.14 4.18	18	NC	
19	GND	5.1	20	NC	
21	SD1_SEL	4.10	22	NC	
23	NC		24	NC	
25	NC		26	NC	
27	NC		28	VSYS	5.1
29	NC		30	NC	
31	NC		32	NC	
33	NC		34	NC	
35	NC		36	NC	
37	GND	5.1	38	NC	
39	NC		40	NC	
41	NC		42	NC	
43	I2C4_SCL GPIO2_10	4.12 4.18	44	NC	
45	NC		46	VSYS	5.1
47	NC		48	NC	
49	I2C4_SDA GPIO2_11	4.12 4.18	50	NC	

51	PWM3.OUT	4.17		52	CSI_DATA22 UART3_CTS PWM4.OUT PWM7.OUT GPIO2_06	4.2 4.11 4.17 4.17 4.18
53	CSI_FIELD ADC1_IN5 ADC2_IN5 GPIO1_05	4.2 4.15 4.15 4.18		54	GPIO5_00	4.18
55	GND	5.1		56	GPIO5_05	4.18
57	NC			58	CSI_DATA13 I2C1_SDA SPI2_CS0_N	4.2 4.12 4.13
59	GPIO5_08	4.18		60	GPIO5_03	4.18
61	CSI_DATA5 SD1_CD_B UART1_RTS GPIO1_19	4.2 4.10 4.11 4.18		62	GPIO5_01	4.18
63	CSI_DATA15 UART5_RX I2C2_SDA SPI2_MISO GPIO1_31	4.2 4.11 4.12 4.13 4.18		64	VSYS	5.1
65	CSI_DATA14 ANATOP.OTG1_ID UART5_TX I2C2_SCL SPI2_MOSI GPIO1_30	4.2 4.8 4.11 4.12 4.13 4.18		66	TS_X+	4.16
67	CSI_DATA4 UART1_CTS GPIO1_18	4.2 4.11 4.18		68	TS_X-	4.16
69	CSI_DATA12 I2C1_SCL SPI2_CLK GPIO1_28	4.2 4.12 4.13 4.18		70	TS_Y+	4.16
71	GND	5.1		72	TS_Y-	4.16
73	CSI_VSYNC UART5_RTS ADC1_IN8 ADC2_IN8 PWM1.OUT GPIO1_08	4.2 4.11 4.15 4.15 4.17 4.18		74	LCD_DATA22 CSI_DATA14 MQS_RIGHT SPI1_MOSI GPIO3_27	4.1 4.2 4.7 4.13 4.18
75	GPIO1_10	4.18		76	LCD_DATA23 CSI_DATA15 MQS_LEFT SPI1_MISO GPIO3_28	4.1 4.2 4.7 4.13 4.18
77	CSI_DATA6 SAI1_TX_SYNC SPI1_CLK GPIO4_25	4.2 4.6 4.13 4.18		78	VSYS	5.1
79	CSI_DATA7 SAI1_TX_BCLK SD1_CD_B SPI1_CS0_N GPIO4_26	4.2 4.6 4.10 4.13 4.18		80	SD1_CLK GPIO2_17	4.10 4.18
81	CSI_MCLK ENET1_MDIO ADC1_IN6 ADC2_IN6 GPIO1_06	4.2 4.3.2 4.15 4.15 4.18		82	USB.OTG1_PWR SD1_CMD GPIO2_16	4.8 4.10 4.18
83	CSI_DATA8 SAI1_RX_DATA GPIO4_27	4.2 4.6 4.18		84	ANATOP.OTG1_ID SD1_DATA_0 CAN BUS1.TX GPIO2_18	4.8 4.10 4.14 4.18
85	CSI_DATA9 SAI1_TX_DATA SPI1_MISO GPIO4_28	4.2 4.6 4.13 4.18		86	SD1_DATA_1 SPI1_MOSI CAN BUS1.RX GPIO2_19	4.10 4.13 4.14 4.18
87	GND	5.1		88	CSI_DATA10 SD1_DATA_2 CAN BUS2.TX GPIO2_20	4.2 4.10 4.14 4.18

89	CSI_DATA4 SAI1_RX_SYNC UART5_RTS SPI2_MOSI GPIO4_23	4.2 4.6 4.11 4.13 4.18		90	SD1_DATA_3 CAN BUS2.RX GPIO2_21	4.10 4.14 4.18
91	CSI_DATA5 SAI1_RX_BCLK UART5_CTS SPI2_MISO GPIO4_24	4.2 4.6 4.11 4.13 4.18		92	LCD_DATA17 UART7_RX GPIO3_22	4.1 4.11 4.18
93	GPIO5_06	4.18		94	LCD_DATA16 CSI_DATA0 UART7_TX GPIO3_21	4.1 4.2 4.11 4.18
95	CSI_PIXCLK UART6_RX I2C1_SCL GPIO4_18	4.2 4.11 4.12 4.18		96	VSYS	5.1
97	CSI_MCLK UART6_TX I2C1_SDA GPIO4_17	4.2 4.11 4.12 4.18		98	LCD_PCLK SAI3_MCLK UART4_TX GPIO3_00	4.1 4.6 4.11 4.18
99	PWM5.OUT PWM6.OUT GPIO1_29 GPIO4_16	4.17 4.17 4.18 4.18		100	LCD_HSYNC SAI3_TX_BCLK UART4_CTS SPI2_CS1_N GPIO3_02	4.1 4.6 4.11 4.13 4.18
101	CSI_DATA2 UART5_TX SPI2_CLK GPIO4_21	4.2 4.11 4.13 4.18		102	LCD_VSYNC SAI3_RX_DATA UART4_RTS SPI2_CS2_N GPIO3_03	4.1 4.6 4.11 4.13 4.18
103	CSI_DATA3 SAI1_MCLK UART5_RX SPI2_CS0_N GPIO4_22	4.2 4.6 4.11 4.13 4.18		104	LCD_DE SAI3_TX_SYNC UART4_RX GPIO3_01	4.1 4.6 4.11 4.18
105	GND	5.1		106	LCD_DATA0 SAI1_MCLK PWM1.OUT GPIO3_04	4.1 4.6 4.17 4.18
107	ENET1_MDC ADC1_IN7 ADC2_IN7 GPIO1_07	4.3.2 4.15 4.15 4.18		108	LCD_DATA1 SAI1_TX_SYNC PWM2.OUT GPIO3_05	4.1 4.6 4.17 4.18
109	CSI_DATA18 ENET1_RX_EN CAN BUS2.TX GPIO2_02	4.2 4.3.2 4.14 4.18		110	LCD_DATA2 SAI1_TX_BCLK I2C4_SDA PWM3.OUT GPIO3_06	4.1 4.6 4.12 4.17 4.18
111	CSI_DATA1 UART3_TX GPIO1_24	4.2 4.11 4.18		112	LCD_DATA3 SAI1_RX_DATA I2C4_SCL PWM4.OUT GPIO3_07	4.1 4.6 4.12 4.17 4.18
113	CSI_VSYNC UART6_RTS I2C2_SDA PWM7.OUT GPIO4_19	4.2 4.11 4.12 4.17 4.18		114	VSYS	5.1
115	CSI_HSYNC UART6_CTS I2C2_SCL PWM8.OUT GPIO4_20	4.2 4.11 4.12 4.17 4.18		116	LCD_DATA4 SAI1_TX_DATA UART8_CTS GPIO3_09	4.1 4.6 4.11 4.18
117	CSI_DATA0 UART3_RX GPIO1_25	4.2 4.11 4.18		118	LCD_DATA5 UART8_RTS SPI1_CS1_N GPIO3_10	4.1 4.11 4.13 4.18
119	CCM_CLK1_P	5.2.2		120	LCD_DATA6 UART7_CTS SPI1_CS2_N GPIO3_11	4.1 4.11 4.13 4.18

121	CCM_CLK1_N	5.2.2		122	LCD_DATA7 UART7_RTS SPI1_CS3_N GPIO3_12	4.1 4.11 4.13 4.18
123	GND	5.1		124	LCD_DATA8 CSI_DATA16 CAN BUS1.TX GPIO3_13	4.1 4.2 4.14 4.18
125	NC			126	LCD_DATA9 CSI_DATA17 SAI3_MCLK CAN BUS1.RX GPIO3_14	4.1 4.2 4.6 4.14 4.18
127	NC			128	LCD_DATA10 CSI_DATA18 SAI3_RX_SYNC CAN BUS2.TX GPIO3_15	4.1 4.2 4.6 4.14 4.18
129	UART1_TX I2C1_SCL ADC1_IN2 ADC2_IN2 GPIO1_02	4.11 4.12 4.15 4.15 4.18		130	LCD_DATA11 CSI_DATA19 SAI3_RX_BCLK CAN BUS2.RX GPIO3_16	4.1 4.2 4.6 4.14 4.18
131	MQS_LEFT I2C2_SDA ADC1_IN1 ADC2_IN1 GPIO1_01	4.7 4.12 4.15 4.15 4.18		132	VSYS	5.1
133	SAI2_MCLK GPIO1_11	4.6 4.18		134	LCD_DATA12 CSI_DATA20 SAI3_TX_SYNC GPIO3_18	4.1 4.2 4.6 4.18
135	UART1_RX I2C1_SDA ADC1_IN3 ADC2_IN3 GPIO1_03	4.11 4.12 4.15 4.15 4.18		136	LCD_DATA13 CSI_DATA21 SAI3_TX_BCLK GPIO3_19	4.1 4.2 4.6 4.18
137	SAI2_TX_BCLK MQS_LEFT PWM6.OUT GPIO1_13	4.6 4.7 4.17 4.18		138	LCD_DATA14 CSI_DATA22 SAI3_RX_DATA GPIO3_20	4.1 4.2 4.6 4.18
139	SAI2_TX_DATA PWM8.OUT GPIO1_15	4.6 4.17 4.18		140	LCD_DATA15 CSI_DATA23 SAI3_TX_DATA	4.1 4.2 4.6
141	GND	5.1		142	LCD_DATA18 PWM5.OUT GPIO3_23	4.1 4.17 4.18
143	SAI2_RX_DATA PWM7.OUT GPIO1_14	4.6 4.17 4.18		144	LCD_DATA19 CSI_DATA11 GPIO3_24	4.1 4.2 4.18
145	SAI2_TX_SYNC MQS_RIGHT GPIO1_12	4.6 4.7 4.18		146	LCD_DATA20 CSI_DATA12 UART8_TX SPI1_CLK GPIO3_25	4.1 4.2 4.11 4.13 4.18
147	NC			148	LCD_DATA21 CSI_DATA13 UART8_RX SPI1_CS0_N GPIO3_26	4.1 4.2 4.11 4.13 4.18
149	NC			150	VSYS	5.1
151	NC			152	GPIO4_14	4.18
153	NC			154	SAI3_TX_DATA SPI2_CS3_N	4.6 4.13
155	NC			156	USB_PWR_EN_B	4.9
157	NC			158	HUB_USB3_D_N	4.9
159	GND	5.1		160	HUB_USB3_D_P	4.9
161	GPIO5_02	4.18		162	OC#_PU	4.9
163	NC			164	HUB_USB2_D_N	4.9
165	ONOFF	5.2.1		166	HUB_USB2_D_P	4.9
167	NC			168	VSYS	5.1
169	NC			170	CPU_USB2_D_N HUB_USB1_D_N	4.8 4.9

171	COLD_RESET_IN	5.3		172	CPU_USB2_D_P HUB_USB1_D_P	4.8 4.9
173	NC			174	MQS_RIGHT ANATOP.OTG1_ID I2C2_SCL ADC1_IN0 ADC2_IN0 GPIO1_00	4.7 4.8 4.12 4.15 4.15 4.18
175	GPIO5_09	4.18		176	USB_OTG1_DP	4.8
177	GND	5.1		178	USB_OTG1_DN	4.8
179	PWM4.OUT	4.17		180	USB.OTG1_VBUS	4.8
181	PMIC_STBY_REQ	5.2.1		182	HUB_USB4_D_P	4.9
183	VCC_RTC	5.1		184	HUB_USB4_D_N	4.9
185	ALT_BOOT	5.4		186	VSYS	5.1
187	NC			188	NC	
189	EEPROM_WP	5.2.3		190	NC	
191	MICBIAS	4.5		192	USB.OTG1_CHD_B	4.8
193	MICIN	4.5		194	CSI_HSYNC UART5_CTS ADC1_IN9 ADC2_IN9 PWM2.OUT GPIO1_09	4.2 4.11 4.15 4.15 4.17 4.18
195	AUD_GND	5.1		196	USB.OTG2_VBUS	
197	RLINEIN	4.5		198	NC	
199	LLINEIN	4.5		200	USB.OTG1_PWR ADC1_IN4 ADC2_IN4 PWM3.OUT GPIO1_04	4.8 4.15 4.15 4.17 4.18
201	RHPOUT	4.5		202	PMIC_ON_REQ	5.2.1
203	LHPOUT	4.5		204	VSYS	5.1

6.2 Mating Connectors

Table 57 Connector type

CL-SOM-iMX6UL connector		Carrier board (mating) connector P/N	
Ref.	Implementation	Mfg.	P/N
P1	2-sides PCB based SODIMM-204 edge connector	Lotes	AAA-DDR-109-K01

6.3 Mechanical Drawings

Figure 3 CL-SOM-iMX6UL Top

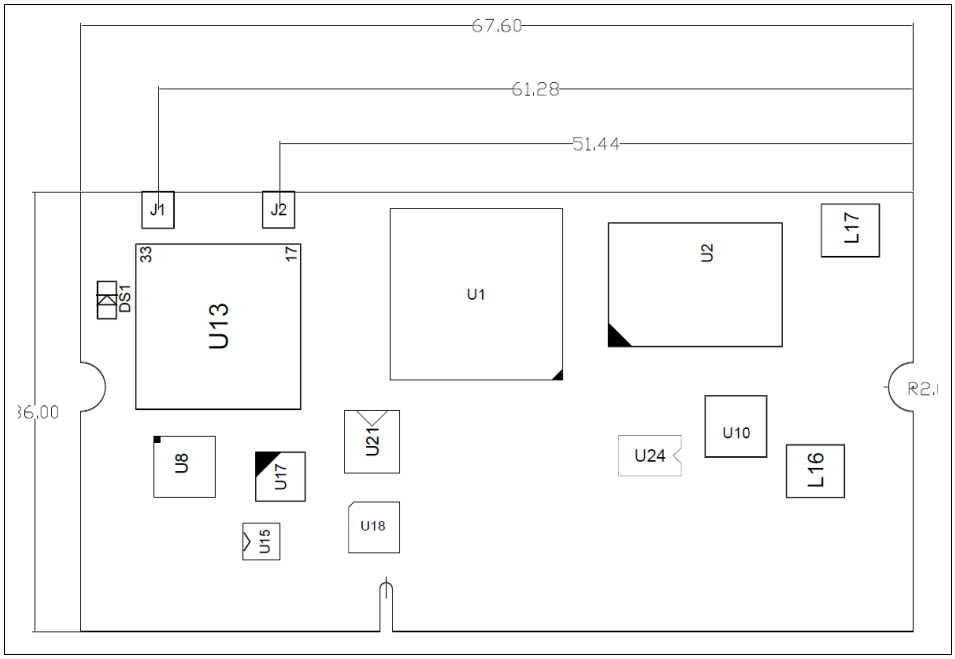
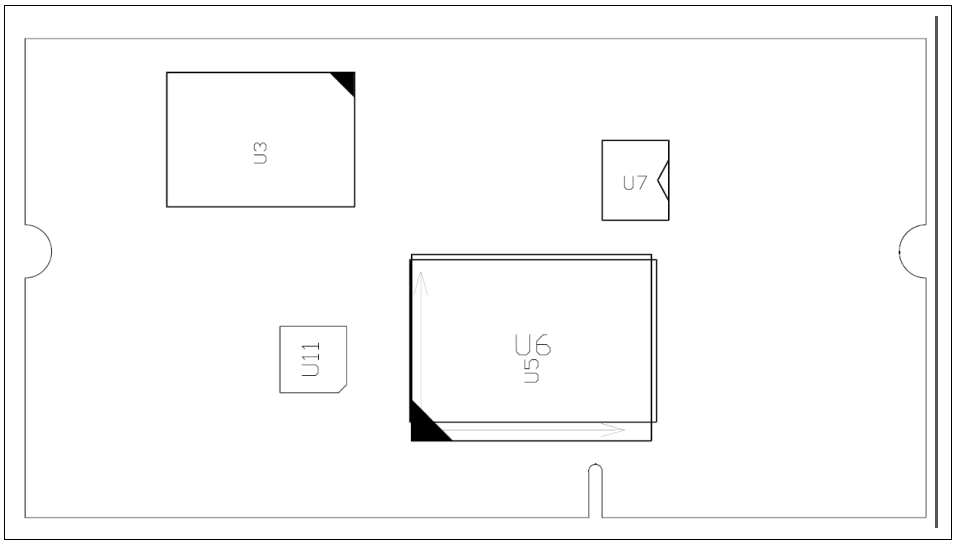


Figure 4 CL-SOM-iMX6UL bottom



1. All dimensions are in millimeters.
2. Height of all components is < 2mm.
3. Baseboard connectors provide 2.8 ± 0.25mm board-to-board clearance.
4. Board thickness is 1.0mm.

Mechanical drawings are available in DXF format at http://www.compulab.com/products/computer-on-modules/cl-som-imx6ul-freescale-imx6-ultralite-system-on-module/#devres

6.4 Standoffs/Spacers

CL-SOM-iMX6UL has two semicircular mounting holes to physically secure the SoM to the carrier board. Secure CL-SOM-iMX6UL to the carrier board by mounting two spacers with any adequate screws and nuts. Spacers must comply with the following specification:

- M2x0.4 thread, 3.0±0.1 mm length

7 OPERATIONAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

Table 58 Absolute Maximum ratings

Parameter	Min	Typ	Max	Unit
Main power supply voltage (VSYS)	-0.3		6	V
USB OTG VBUS (USB_OTGX_VBUS)	0		5.5	V
Voltage on any non-power supply pin	-0.5		3.6	V

NOTE: Exceeding the absolute maximum ratings may damage the device.

7.2 Recommended Operating Conditions

Table 59 Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Main power supply voltage (VSYS)	3.2	5.0	5.5	V
Backup battery supply voltage (V3_COIN)	1.4	3.0	5.5	V
VBUS_5V_OTG		5		V

7.3 DC Electrical Characteristics

Table 60 DC Electrical Characteristics

Parameter	Min	Typ	Max	Unit
V_{OH}	3.05			V
V_{OL}			0.15	V
V_{IH}	2.38		3.3	V
V_{IL}	0		0.96	V

7.4 ESD Performance

Table 61 ESD Performance

Interface	ESD Performance
iMX6UL pins	2kV Human Body Model (HBM), 500V Charge Device Model (CDM)
USB Hub pins (UH option)	5kV Human Body Model (HBM)
LVDS (L option)	2kV Human Body Model (HBM)

7.5 Operating Temperature Ranges

The CL-SOM-iMX6UL is available with three options of operating temperature range.

Table 62 CL-SOM-iMX6UL Temperature Range Options

Range	Temp.	Description
Commercial	0º to 70º C	Sample boards from each batch are tested for the lower and upper temperature limits. Individual boards are not tested.
Extended	-20º to 70º C	Every board undergoes a short test for the lower limit (-20º C) qualification.
Industrial	-40º to 85º C	Every board is extensively tested for both lower and upper limits and at several midpoints.

8 APPLICATION NOTES

8.1 Carrier Board Design Guidelines

- Ensure that all VSYS and GND power pins are connected.
- Major power rails - VSYS and GND must be implemented by planes, rather than traces. Using at least two planes is essential to ensure the system signal quality, because the planes provide a current return path for all interface signals.
- It is recommended to put several 100nF and 10/100uF capacitors between VSYS and GND near the mating connectors.
- It is recommended to connect the standoff holes of the carrier board to GND, in order to improve EMC.
- Except for a power connection, no other connection is mandatory for CL-SOM-iMX6UL operation. All power-up circuitry and all required pullups/pulldowns are available onboard CL-SOM-iMX6UL.
- If for some reason you decide to place an external pullup or pulldown resistor on a certain signal (for example - on the GPIOs), first check the documentation of that signal provided in this manual. Certain signals have on-board pullup/pulldown resistors required for proper initialization. Overriding their values by external components will disable board operation.
- You must be familiar with signal interconnection design rules. There are many sensitive groups of signals. For example:
  - Ethernet, SATA, USB and more signals must be routed in differential pairs and by a controlled impedance trace.
  - Audio input must be decoupled from possible sources of carrier board noise.
- Be careful when placing components under the CL-SOM-iMX6UL module. The carrier board interface connector provides 1mm mating height. Bear in mind that there are components on the underside of the CL-SOM-iMX6UL.
- Refer to the SB-SOM-iMX6UL carrier board reference design schematics.

8.2 Carrier Board Troubleshooting

- Using grease solvent and a soft brush, clean the contacts of the mating connectors of both the module and the carrier board. Remnants of soldering paste can prevent proper contact. Take care to let the connectors and the module dry entirely before re-applying power – otherwise corrosion may occur.
- Using an oscilloscope, check the voltage levels and quality of the VSYS power supply. It should be as specified in section 7.2. Check that there is no excessive ripple or glitches. First perform the measurements without plugging in the module. Then plug in the module and measure again. Measurement should be performed on the pins of the mating connector.
- Using an oscilloscope, verify that the GND pins of the mating connector are indeed at zero voltage level and that there is no ground bouncing. The module must be plugged in during the test.
- Create a "minimum system" - only power, mating connectors, the module and a serial interface.
- Check if the system starts properly. In system larger than the minimum, possible sources of disturbance could be:
- Devices improperly driving the local bus
- External pullup/pulldown resistors overriding the module on-board values, or any other component creating the same "overriding" effect

- Faulty power supply
- In order to avoid possible sources of disturbance, it is strongly recommended to start with a minimal system and then to add/activate off-board devices one by one.
- Check for the existence of soldering shorts between pins of mating connectors. Even if the signals are not used on the carrier board, shorting them on the connectors can disable the module operation. An initial check can be performed using a microscope. However, if microscope inspection finds nothing, it is advisable to check using an X-ray, because often solder bridges are deep beneath the connector body. Note that solder shorts are the most probable factor to prevent a module from booting.
- Check possible signal short circuits due to errors in carrier board PCB design or assembly.
- Improper functioning of a customer carrier board can accidentally delete boot-up code from CL-SOM-iMX6UL, or even damage the module hardware permanently. Before every new attempt of activation, check that your module is still functional with CompuLab SB-SOM-iMX6UL carrier board.
- It is recommended to assemble more than one carrier board for prototyping, in order to ease resolution of problems related to specific board assembly.

8.3 Ethernet Magnetics Implementation

8.3.1 Magnetics Selection

Refer to the table below for compatible magnetics. The list of "Qualified Magnetics" contains magnetics recommended by Micrel. Designers should test and qualify all magnetics before using them in an application.

Table 63 Qualified Magnetics

Vendor	P/N	Auto MDI-X
Bel Fuse	558-5999-U	YES
Bel Fuse	SI-46001	YES
Bel Fuse	SI-50170	YES
Delta	LF8505	YES
LanKom	LF-H41S	YES
Pulse	H1102	YES
Pulse (low-cost)	H1260	YES
Transpower	HB726	YES

8.3.2 Magnetics Connection

For magnetic modules connection, please refer to the SB-SOM-iMX6UL reference design schematics